A Novel Control Technique for Power Factor Correction in SEPIC Converter Utilizing Input/Output Voltage Waveforms Sampling

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Abstract—In this study, a simple and novel control technique for Power Factor Correction (PFC) is introduced, which is a SEPIC-based (Single-ended Primary-inductor Converter based) rectifier with high input power factor. Operation of the proposed method is based on sampling of input and output voltages in SEPIC rectifier. Using samples of input and output voltage, this control system makes the input current to follow a sinusoidal path. As a result, the line current’s Total Harmonic Distortion (THD) is reduced and the input power factor is improved. This paper also compares the new method with the conventional control method for the power factor correction. In order to examine the proposed control technique comprehensively, computer simulations and experimental implementations were utilized to verify the feasibility and effectiveness of this novel control technique.

Keywords—Power Factor Correction; SEPIC Rectifier; Total Harmonic Distortion; Single-ended Primary-inductor Converter; Input Power Factor

I. INTRODUCTION

Vast and growing use of AC to DC converters caused significant attention toward their implementation and operation problems. One of these major problems is the harmonic content in the input current, resulted by poor performance of the converters in terms of input power factor. A variety of active and passive Power Factor Correction (PFC) techniques were implemented to compensate the input current’s harmonic content [1-3]. One of the simplest methods is using filters, which is in fact one of the passive PFC methods [4]. Passive PFC methods are more expensive, and their larger components make them more inappropriate for implementation and less effective in comparison with the active PFC methods.

Active PFC techniques seek the unity power factor by applying different switching topologies [5-9]. They mostly utilize a suitable DC-DC converter to increase the power factor. The increased use of converters led to introduction of new methods and topologies to improve their performance [10]. In [11] an interleaved topology of DC-DC converter is investigated, which can be used for PFC. Active PFC techniques manage to control and shape the input current waveform in the way that it becomes similar to the input voltage waveform (close to a perfect sinusoidal wave).

Some problems occur, regarding the operation of switching power supplies. One of such problems is generation of electromagnetic noise, and its effect on other equipment in surrounding environment. These types of problems mainly arise due to the non-linear nature of operation of these types of power supplies [12]. The concept of power quality can be described as an overall optimal and satisfactory operation and performance of these systems, in terms of a set of parameter values, such as input waveforms’ harmonic content. Many standards and restrictions were created to adjust setting of limitations to the amount of harmonic distortion in order to increase the power quality. One of the good power quality measures is the amount of power factor (P.F). The P.F is described as the ratio of real power flowing into the load, over the apparent power, as it is shown in (1).

\[
P.F = \frac{P}{S} = \frac{P_{in}}{E_{rms} \cdot I_{rms}}
\]

(1)

Power factor value changes between 0 and 1. Two main factors affect the amount of power factor: phase difference between the current and voltage waveforms, which results in the product value of \( I_{rms} \) and \( V_{rms} \) to become higher than \( P_{in} \) and therefore, the power factor value declines to lower than unity; and presence of harmonic content in the current waveform, which increases the \( I_{rms} \) value, and therefore declines the power factor value. Mathematically, power factor can be described as the product of displacement and distortion factors as (2).

\[
P.F = \frac{\cos \varphi}{\sqrt{1 + THD^2}}
\]

(2)

in which \( \varphi \) is the phase difference between the voltage and current waveforms and \( THD \) is the total harmonic distortion.

To decrease the amount of total harmonic distortion (THD), and subsequently, to increase the amount of power factor, different converter topologies were implemented; among them are Boost, Buck, Buck-Boost and Multilevel converters.

Many converter topologies and control strategies are introduced in the literature to perform this important task. Different aspects in terms of the design and operation of
the circuitry are thoroughly discussed in [13]. Also various control techniques are introduced in literature in order to reach the unity power factor – the average current mode, peak current mode, hysteresis control and some other techniques [13] – and their details, features and usage circumstances are presented and discussed [14,15]. Single-ended primary-inductor converter (SEPIC) is a popular converter topology which is being used for power factor correction tasks in single phase rectification [16,17]. This type of converters is the basis of the study presented in this paper. But initially, it is noteworthy to discuss important factors regarding the choice of proper converter topologies for different applications. Limitations, considering the amount of input power factor and THD (input power quality) are: type of output DC voltage (constant or variable), power flow direction (unidirectional or bidirectional), cost of implementation, size, weight, efficiency, etc.

A perfect rectifier, in which an appropriate power factor correction scheme is implemented, shows the same characteristics as a resistive load. Main features of active power factor correction techniques are reduction in input current harmonics, decline in power losses and relatively smaller size of the converter circuit and input filters.

A conventional method of implementing PFC in bridge rectifiers is using a SEPIC converter, with an average current mode (ACM) control scheme. In this paper, along with discussing the performance of the conventional active PFC using a SEPIC rectifier and average current mode control scheme, a novel method of PFC, based on the SEPIC converter is introduced. First, the control scheme and implementation of this novel PFC method is described. Then, based on the data acquired through computer simulations and laboratory experiments, the operation and performance of the new technique is compared with the conventional ACM technique. At the end, the performance of the new method is evaluated.

This paper is organized as follows: the single-ended primary-inductor converter topology is reviewed in Section II; conventional PFC methods are presented in Section III; Section IV deals with the proposed SEPIC rectifier PFC method; in Section V, both conventional average current PFC method and the new proposed method of this study are investigated using computer simulations; experimental circuit prototypes are implemented and investigated for both the conventional and proposed PFC methods in Section VI; finally, some concluding remarks are provided in Section VII.

II. SINGLE-ENDED PRIMARY-INDUCTOR CONVERTER

Single-ended primary-inductor converter (SEPIC) is a DC-DC converter topology which allows the output voltage to be greater than, less than, or equal to its input terminal. Output voltage in SEPIC is controlled by switching duty cycle [18].

Considering Fig. 1, during the steady-state operation of SEPIC, the average voltage along the capacitor \( C_1 \) (\( V_{C1} \)) is equal to the input voltage \( (V_{in}) \). The capacitor \( C_1 \) does not allow direct current, therefore, the average current across it \( (I_{C1}) \) is equal to zero, so the inductor \( L_2 \) is the only available source for the load current. The amount of average current across the inductor \( L_2 \) \( (I_{L2}) \) is the same as the load current and therefore, is independent of the input voltage.

Considering the voltages in Fig. 1, we have:

\[
V_{in} = V_{L1} + V_{C1} + V_{L2}. \tag{3}
\]

Due to the fact that the average of \( V_{C1} \) is equal to \( V_{in} \) we have \( V_{L1} = -V_{L2} \), thus it is possible to wind the two inductors on the same core – since the voltages are equal, the effect of their mutual inductance will be zero, assuming correct winding polarity. Again, since voltages have the same magnitude, the ripple currents of the inductors will have the same magnitudes.

Considering the currents in Fig. 1, we have:

\[
I_{D1} = I_{L1} - I_{L2}. \tag{4}
\]

When switch \( S_1 \) turns on, current \( I_{L1} \) increases, while current \( I_{L2} \) increases in negative direction, as it is illustrated in Fig. 1(a). The input source supplies the energy needed to increase \( I_{L1} \). Since the instantaneous voltage \( V_{C1} \) is approximately equal to \( V_{in} \), the voltage \( V_{L1} \) would be near \( -V_{in} \). Consequently, the capacitor \( C_1 \) is the energy supplier for increasing the current in \( I_{L2} \) and therefore, the total energy stored in inductor \( L_2 \).

When switch \( S_1 \) turns off, current \( I_{C1} \) becomes equal to the current \( I_{L1} \), because the inductors do not allow instantaneous variations in current. The current \( I_{L2} \) never reverses direction and therefore, continues in the negative direction. It can be observed from Fig. 1(b) that a negative \( I_{L2} \) is added to the current \( I_{L1} \) which increases current delivery to the load. Using Kirchhoff’s Current Law, it is concluded that \( I_{D1} = I_{C1} - I_{L2} \). Also, while the switch \( S_1 \) is off, power delivery to the load is through both \( L_2 \) and \( L_1 \). Capacitor \( C_1 \) is charged by \( L_2 \) in the duration in which the switch is off, and \( C_1 \) charges \( L_1 \) in the duration in which the switch is on.

III. REVIEW OF THE CONVENTIONAL PFC METHODS

If we consider both voltage and current waveforms as perfect sinusoidal waves, then for the power factor value we have:

\[
P.F = \cos \varphi \tag{5}
\]
in which, $\varphi$ is the phase difference between the voltage and current and the term $\cos \varphi$ is called “harmonic displacement factor”. In the case of a non-perfect current waveform, (5) changes to:

$$P.F = K_p \cos \varphi$$

in which $K_p$ is defined as:

$$K_p = \frac{1}{\sqrt{1+THD^2}}, \quad K_p \in [0,1].$$

Therefore, the amount of power factor is influenced by variations in the harmonic displacement factor and the amount of total harmonic distortion. Consequently, the practical way of implementing power factor correction is to reduce the input current’s THD, which increases P.F value, according to (7). This means that the input current should be controlled in appropriate manner and this makes the basis of a power factor correction method.

The main idea behind the implementation of average current mode power factor correction based on a diode bridge rectifier and DC-DC converter is presented in Fig. 2.

**Average current mode PFC control method**

Different circuitries were introduced to the date to fulfill the task of PFC in rectifiers. Among these circuits, one of the most popular is based on Single-ended primary-inductor converter (SEPIC), which is illustrated in Fig. 3. A conventional control scheme for this circuit is the average current mode technique, which has the most extensive usage in power factor correction applications due to its easy implementation, simple use and good performance. A PFC controller IC, based on the ACM scheme is introduced by Texas Instruments with the UC1854 family in early 1990s.

The average current mode control method has two main duties in performing the power factor correction in a SEPIC rectifier circuit: adjusting the input current waveform in a manner that the PFC is achieved; and adjusting the output voltage which is applied to the load, using appropriate changes in the switching duty cycle. The average current mode control scheme is based on controlling the inductor current by a current feedback loop, in a manner that the current is forced to track a predefined reference current. This predefined reference current is determined using the following equation:

$$I_{ref}(t) = \frac{V_{cont} \cdot V_{in}(t)}{V_{rms}}$$

in which, $V_{in}(t)$ is the rectified voltage of the diode bridge, $V_{cont}$ is the scaling factor, influenced by the output voltage control loop, and $V_{rms}$ is the rms value of the input voltage. From (8) it can be concluded that the shape of $I_{ref}(t)$ waveform is proportional to the voltage $V_{in}(t)$, therefore power factor correction is performed due to the fact that the inductor current is also forced to track the reference current. Fig. 3 presents SEPIC rectifier and control circuitry based on IC UC3854.

**IV. THE PROPOSED SEPIC RECTIFIER PFC METHOD**

In this study, a new control scheme is introduced for implementation of power factor correction in SEPIC rectifiers, which is capable of maintaining near unity power factor and improving the THD. The new technique is based on sampling the input and output voltages, $V_{in}$ and $V_{out}$, and uses a compare process over the input voltage which is the basis of generation of the switch’s PWM control signal.

Using two appropriate resistors in series – as it is illustrated in Fig. 4 – desired sampling can be performed from the input voltage, which in fact is the voltage $V_2$ and is sensed through the resistor $R_s$. Considering Fig. 4, the resistor $R_s$ samples the output current of the diode bridge and therefore the voltage, $V_{R_s}$ is proportional to this current. Now if $V_2$ is considered as illustrated in Fig. 4, then the following can be deduced:

$$V_p = V_2 + V_{R_s}.$$
sampling resistors are adjusted appropriately, then the value of $V_3$ must maintain a value exactly equal to zero at all times. This is the basis for operation of the novel method.

Fig. 5 shows the diagram of the SEPIC rectifier along with the new control scheme. Fig. 5 shows that the voltage $V_3$ is first compared with zero. This generates the feed-forward loop which is the main step toward generation of PWM pulse for the switch. As mentioned before, when the input current waveform is a perfect sinusoidal waveform, by choosing appropriate resistor values for $R_1$ and $R_2$, the voltage $V_3$ is accurately tuned to be zero. Therefore, when value of the current – sampled by resistor $R_s$ – begins to change from the desired path (the perfect path which results in a perfect sinusoidal input current waveform), this apparently affects the value of the voltage $V_3$, considering (9). Moreover, considering the current direction, the voltage $V_{Rs}$ is negative in (9), therefore when the current passing through resistor $R_s$ decreases from the desired value, the voltage $V_3$ becomes slightly positive. This turns the comparator, or $D_1(t)$, to “high”. Therefore, if the comparator is considered as a reference for generating the command pulse of the switch, when $D_1(t)$ turns high, the switch turns on and this causes the input current to rise again; consequently, the current sensed through the resistor $R_s$ will rise. The switch maintains its “on” state, until the voltage $V_3$ turns negative – which is a sign that the current is slightly higher than the desired value – and turns $D_1(t)$ to “low” state, and consequently causes the switch to turn off. The behavior of $D_1(t)$ in the moment of changes in the value of $V_3$ is determined by the following:

$$D_1(t) = \begin{cases} V_{CC} & V_3 > 0 \\ 0 & V_3 \leq 0 \end{cases}$$  \hfill (10)

This process can effectively correct the deviation of the input current from its desired sinusoidal waveform path. In fact, considering (10), when the current decreases to lower than desired value, the switch turns on, and consequently increases the amount of current, and when the current increases to higher than the desired value, the switch turns off to decrease the amount of current; therefore, the method can theoretically maintain the input current in a desired sinusoidal waveform through the time.

In order to control the output voltage level of the rectifier, a conventional output voltage feedback controller is implemented, which is presented in Fig. 4. The voltage feedback controller is made of inverter, carrier signal, output voltage reference and voltage divider through resistors $R_3$ and $R_4$. By changing the ratio of these two resistors, it is possible to tune the desired voltage in the output. The output voltage is sampled through these two resistors, then inverted and fed into the integrators input. The integrator resets at the beginning of each switching cycle and results in generation of the carrier signal. Therefore, the carrier signal at the output of the integrator is generated proportional to the output voltage level. Considering Fig. 5, slope of the ramp can be obtained through the following:

$$s = \frac{R_4R_6}{R_4R_6 + R_3 + R_4} V_{out}$$.  \hfill (11)

This signal is then fed into a comparator, along with the output of the comparator, $D_1(t)$ in the feed forward control loop, which compares the $V_3$ voltage level with zero. This process compares and adjusts the duty cycle of the PWM control signal of the switch in the way that maintains the desirable output voltage level. According to (11), when the output voltage increases to a larger value than desired, slope of the ramp in the carrier signal slightly increases and therefore the comparator decreases the PWM pulse width, resulting in the output voltage to decrease; in contrast, when the output voltage decreases to smaller value than desired, the comparator increases the PWM pulse width to increase the output voltage level. The basis of this output voltage control technique is presented in Fig. 6. Finally, considering Fig. 5, PWM command signal of the switch is obtained as:

$$D(t) = \begin{cases} \text{on} & D_1(t) > D_2(t) \\ \text{off} & D_1(t) \leq D_2(t) \end{cases}.$$.  \hfill (12)

V. SIMULATIONS

We investigated both conventional SEPIC rectifier PFC control technique and the novel proposed method using computer simulations. The simulations were performed in
PSIM environment and the presented results show the behavior of both methods.

Fig. 7(a) illustrates the input current $I_{in}$ time-domain waveform along with the voltage waveform $V_{in}$, for the conventional method resulted through the simulations. The obtained value of power factor for these simulations is equal to 1.0, and the THD value is 6%. The produced output DC voltage, $V_{out}$ is also presented in Fig. 7(b).

The circuit component values used in simulation of the proposed PFC method are: $V_{in} = 32V$, $L_1 = 2mH$, $C_f = 0.82\mu F$, $C_{out} = 1.2mF$, $R_1 = 60k\Omega$, $R_2 = 580\Omega$, $R_3 = 3k\Omega$, $R_4 = 500\Omega$, $R_5 = R_6 = 3.5k\Omega$, $R_7 = 25\Omega$ and the working switching frequency is fixed at 40 kHz.

Fig. 8(a) illustrates the input current $I_{in}$ time-domain waveform along with the input voltage waveform $V_{in}$, for the novel PFC method of this study, obtained through simulations. The calculated value for power factor of these simulations is also equal to 1.0, and the resulted THD is 1.5% which is significantly less than the conventional method. The produced output DC voltage $V_{out}$ for this simulation is presented in Fig. 8(b).

VI. EXPERIMENTAL VERIFICATION

We constructed experimental circuit prototypes in laboratory for both the conventional and proposed PFC methods to investigate the expected results from the proposed SEPIC rectifier power factor correction control scheme, and to make a reliable evaluation and comparison between the performance of both proposed and conventional ACM methods. Circuit of the conventional ACM method is accomplished using IC UC3854, according to the schematic diagram of Fig. 3.

The input voltage and current waveforms resulted from experimental implementation of the conventional ACM and the novel proposed power factor correction methods are presented in Fig. 9 and Fig. 10 respectively.

The results of simulations and laboratory experiments, for both of the conventional SEPIC rectifier power factor correction method based on the IC UC3854 and the new proposed method of this study are presented in Table 1.

<table>
<thead>
<tr>
<th>Simulation and Experimental Results</th>
<th>Simulations</th>
<th>Laboratory Experiments</th>
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<tbody>
<tr>
<td><strong>Conventional PFC method</strong> based on IC UC3854</td>
<td><strong>Proposed PFC method of this study</strong></td>
<td><strong>Conventional PFC method</strong> based on IC UC3854</td>
</tr>
<tr>
<td>cos $\varphi$</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>THD</td>
<td>6%</td>
<td>1.5%</td>
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</table>
The table gives an excellent comparison between the results. It shows that the results of the proposed method are better than the conventional method. THD value is reduced from 11.7% in the conventional PFC method to 5.7% in the proposed method in experimental setup, and therefore the novel proposed PFC method proves feasible with significantly better results. Moreover, there is a good agreement between the results obtained by simulation and laboratory experiments. The slight differences between computer simulations and laboratory experiments are due to the ideal consideration of components in simulations.

VII. CONCLUSION

In this study, we introduced a simple and novel control scheme for power factor correction based on single-ended primary-inductor converter (SEPIC) rectifiers, which is capable of maintaining high input power factor and improving THD. The method is based on sampling input and output voltage waveforms, and uses a simple comparison technique on sampled input voltage, to produce the PWM control signal of the switch, which results in much better performance in terms of maintaining high power factor and reduction of the THD value. To evaluate the operation and performance of the proposed method more effectively, we compared its performance with a conventional active SEPIC rectifier power factor correction method, implemented using the IC UC3854. We simulated and constructed the circuits for both methods. The results show better steady state and transient performance of the proposed method with respect to the conventional method, moreover, the simulations and experimental results match closely. According to the simulation results, THD value using the conventional PFC method is 6%, while it reduces to 1.5% in the proposed method. Also, according to the experimental results, the THD value using the conventional PFC method is 11.7%, while it reaches 5.7% using the novel technique. Both results support the superior performance of the proposed method of this study over the conventional technique. Experimental results in this study show that the new technique can successfully maintain the sinusoidal waveform of the input current with a power factor value, close to unity.

REFERENCES