STM JOURNALS

Journal of Electronic Design Technology
ISSN: 2229-6980
Volume 5, Issue 1
www.stmjournals.com

Improvement of Design Issues in FinFET based Design Techniques for XOR and XNOR Circuits at 45 nm Technology

Neha Yadav*[1], *Ashish Kumar Singhal*[2]
[1]Research Scholar of ITM University, India
[2]Department of EE, SR group of Institution, Jhansi (U.P), India

Abstract

The scaling of conventional CMOS circuit inclines to the short channel effect due to leakage current increase in the circuit. To minimize the short channel effect, FINFET can be used in place of conventional CMOS circuits. This paper demonstrates comparative performance study of high speed, low power and low voltage on XOR and XNOR digital circuit. This paper assesses and compares the performance of XOR and XNOR logic circuits. This comparison is based on analysis of various design technique for XOR and XNOR logic circuits. The performances of XOR and XNOR circuits are based on CADANCE VIRTUOSO tool at voltage supply 0.6 voltages and the temperature is 26^0C and all the simulation results have been generated by Cadence SPECTRE simulator at 45 nm technology. The XOR and XNOR circuits with pass transistor, inverter based design, transmission gate and with feedback transistors designs are desirable for arithmetic circuits. Simulation results reveal low power, delay, power, delay product (PDP), average dynamic power consumption and energy delay product (EDP).

Keywords: *XOR, XNOR, PDP, low power, high speed, pass transistor, transmission gate, feedback circuit cadence SPECTRE simulator at 45 nm technology*

****Author for Correspondence*** E-mail: ashishee@gmail.com

INTRODUCTION

In the last decade semiconductor industry has found an explosive growth of into multimedia based applications as seen with cell phones, laptops, sensors, smart card and many other applications. The growth of semiconductor industry is driving the designers to strain for smaller silicon area, longer battery life, higher speed and dependability [1]. As the CMOS device technology shrinks, the critical worries have been arising with increasing leakage power consumption. The scaling of devices down aims at increasing operational speed, reduction in space used and better control on channel by the gate configurations. The scaling of CMOS technology is based on Moore's law which says that number of transistors on a chip doubles every 17 months.

The scaling of the device is confronting many challenges due to shrinking geometries, lower supply voltage, and higher frequencies, all having a negative impact on device [2]. However, scaling of MOS becomes considerably difficult for technology nodes below 45 nm, where the proximity source and drain reduces the control of the gate over the channel leading to unacceptable short channel effects [3].To reduce short channel effect problem in MOS devices FinFET transistors are used. FinFET transistors are successfully substituting CMOS transistors beyond 22 nm technology node [3]. FinFET is a double gate device in which second gate is added opposite to the first gate, has long been discerned for it's better control on short channel effect [4]. Fabrications of FinFET devices are same as CMOS devices [5]. FinFET can be classified into two categories 1) Independent gate FinFET (IG FinFET), 2) Short gate FinFET (SG FinFET) [6]. In this paper short gate FinFET is used. XOR –XNOR circuits are the sub-circuits that are mostly used in various circuit especially-Arithmetic circuits (Full adder and multipliers), Compressors, Comparators, Parity Checkers, Code

converters, Error-detecting or Error-correcting codes and Phase detector. The performance of complex logic circuit is enhanced by the individual performance of the XOR-XNOR circuits [7,8]. Several designs are available to realize the XOR-XNOR function using different logic styles [9].

The proper selection of XOR-XNOR circuit can add to the performance of large number of circuits. It optimizes the design for reduced delay, lesser PDP and lesser degradation on output voltage level. The aim to design XOR-XNOR gate is to obtain low power consumption and delay in the critical path and full output voltage swing with less number of transistors to implement it [10].
Exclusive–OR (XOR) and Exclusive-NOR (XNOR) circuits have complementary functions with respect to each other. The binary operations that perform the following Boolean Functions-
$A \oplus B = A'B + AB'$
$A \odot B = A'B' + AB$

REVIEW OF VARIOUS XOR AND XNOR CIRCUIT DESIGN OF DIFFERENT FINFET LOGIC STYLES

A. Static FINFET XOR and XNOR Circuit

Complementary circuit uses dual network to implement XOR-XNOR circuit [11-13]. The first part of circuit consists only of complementary pull-up network, while second part is pull-down NMOS network. This is a popular technique and produce results that are widely accepted. Static FinFET XOR-XNOR gate are shown in Figure 1(a), and Figure 1(b). The circuit can be operated with full output voltage. The FinFET XOR gate shows in Figure 1 (a), where A and B are inputs and output is A XOR B. FinFET based XNOR gate shows in Figure 1(b), where A and B is inputs and output is A XNOR B.

Substitute realization of static XOR and XNOR circuit using complementary FinFET transistors and over input- output relation is shown in Figure 1(c). The output waveform of Figure 1(a) and Figure 1(c) shows in Figure 2.
$Z = A \oplus B = (A + B).(A' + B')$
$Z' = (A \oplus B)' = \{(A + B) . (A' + B')\}'$
$Z' = AB + A'B'$
$Z = (AB + A'B')' = A \oplus B$

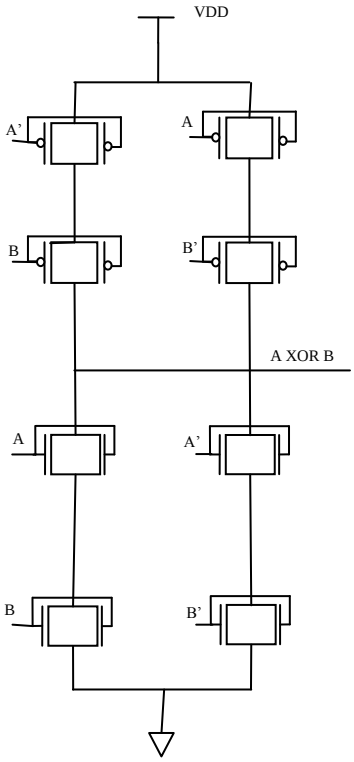


Fig. 1(a)

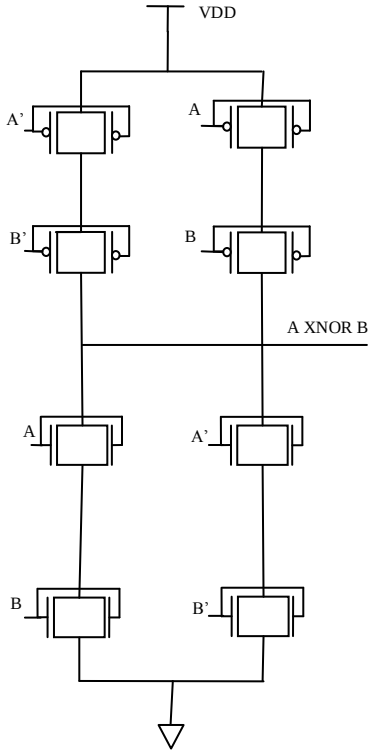


Fig. 1 (b)

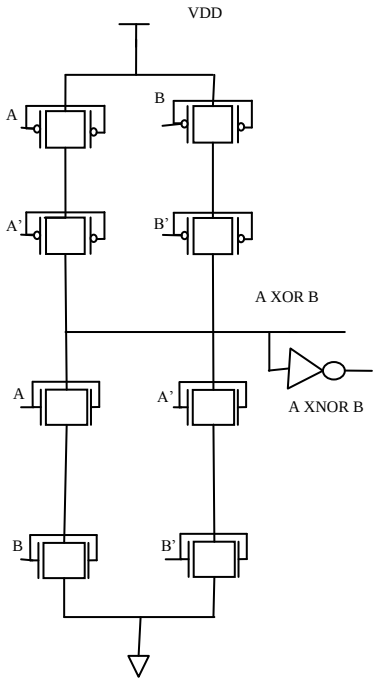
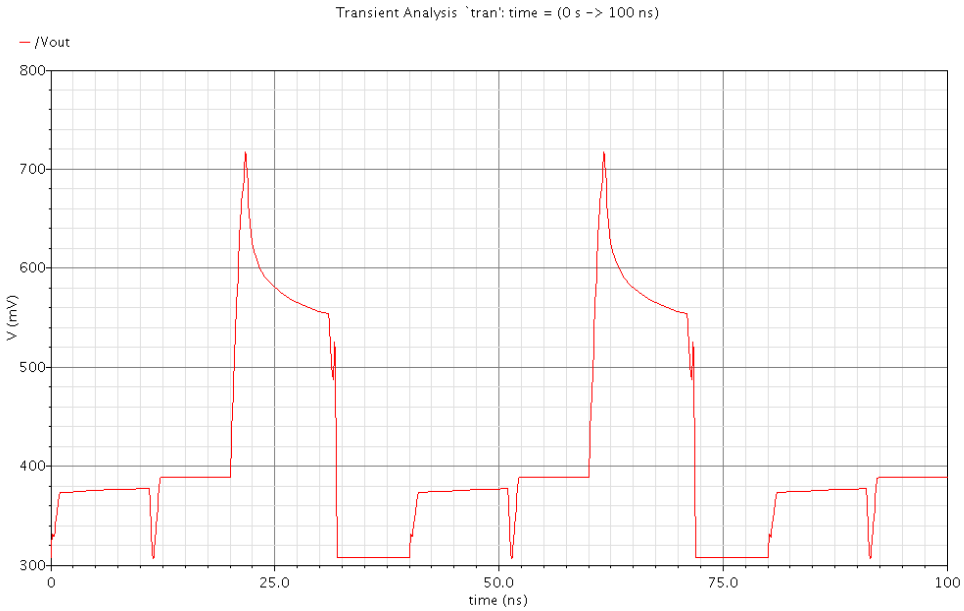


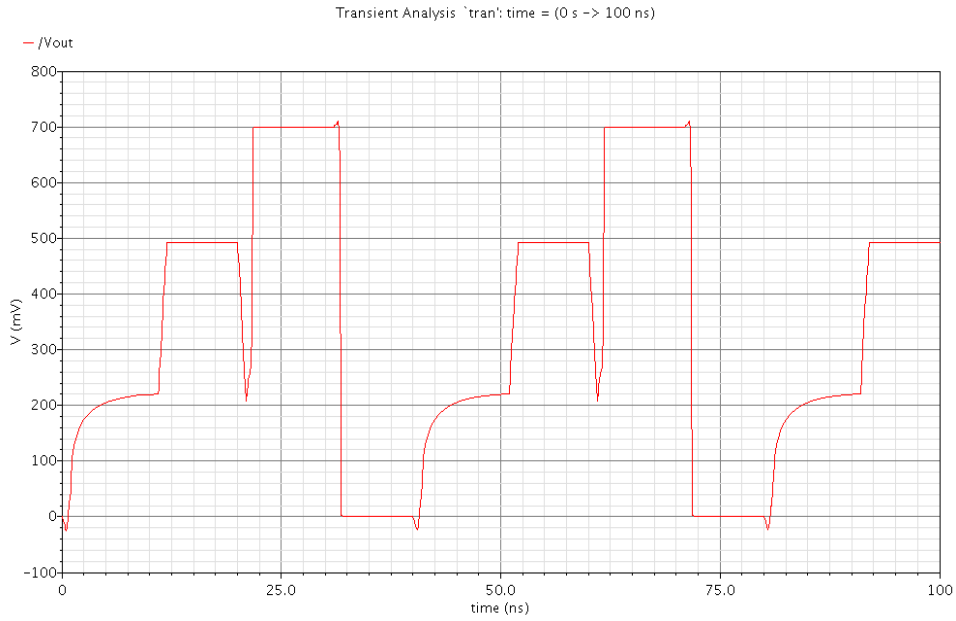
Fig. 1: (c)
Fig. 1 (a–c): *Static FinFET XOR-XNOR Gate.*



Graph 1: *Output Waveform of Fig. 1(a).*

B. Inverter based XOR and XNOR Circuits

Inverter based XOR-XNOR circuits [13] are shown in Figure 2(a) and Figure 2 (b). These circuits are designed by cascading three inverters. There is some limitation of this circuit; one of those circuits has non full voltage swing at the internal nodes of the circuit. However this circuit is operated at a high supply voltage. The study of these cases for the input signals A and B, the output of inverter is nearly an XOR/XNOR function. When A = "High," A' must be "Low", and on the other hand, when A = "Low," A' must be "High." The outputs of XOR-XNOR circuit are shown in Table 1, at low supply voltage 0.6v.



Graph 2: *Output Waveform of Fig. 1(c).*

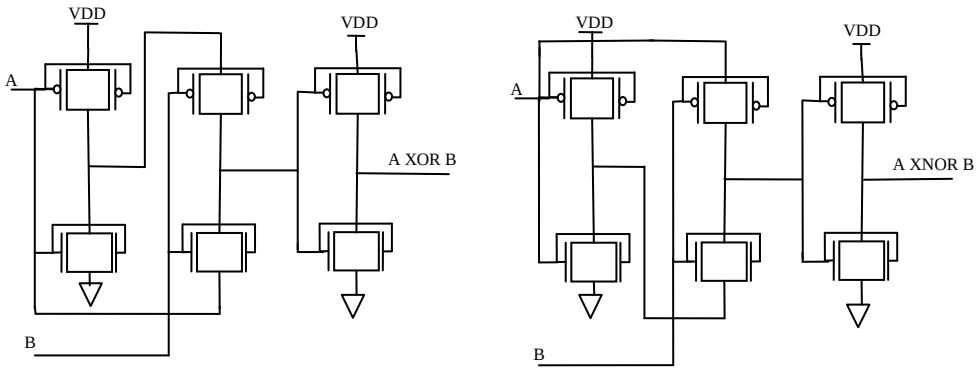


Fig. 2(a) **Fig. 2(b)**

Fig. 2: *Inverter based XOR-XNOR Circuits.*

Table 1: *Input and Output Values For the Fig.2(A) and Fig. 2(B).*

Input		**Output**	
A	***B***	***XOR***	***XNOR***
0	0	Bad 1	Good 0
0	1	Good 0	Good 1
1	0	Good 0	Good 1
1	1	Good 1	Good 0

C. PTL based XOR and XNOR Circuits

Another logic style is Pass Transistor Logic (PTL), it is ordinarily used. Pass transistor logic has been considered a low power logic [14,15].Pass transistor is well-suited to circuits that contain large proportions of XOR gates and arithmetic units, because PTL based implementations of these functions are more effective then CMOS implementations [16]. There are two main pass transistor logic styles [17] one of those uses NMOS only pass-transistor circuits, such as Complementary pass transistor logic (CPL) [18,19] and other one uses both NMOS and PMOS pass-transistors, such as double pass transistor logic (DPL) [20] and DVL [21] . Several XOR-XNOR circuits are shown in Figure 3, which are based on high functionality of the pass transistor logic style. PTL is useful in reduction of output voltage swing, power consumption. This may lead to slow switching in case of a cascade operation such as ripple carry adder.

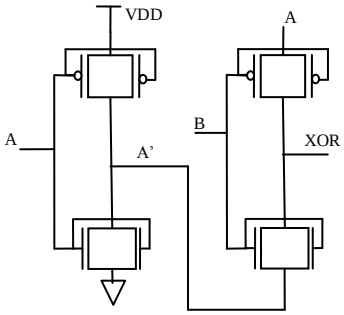


Fig. 3(a)

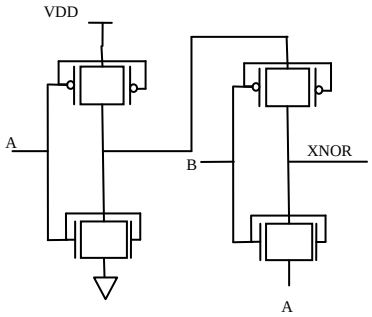


Fig.3 (b)

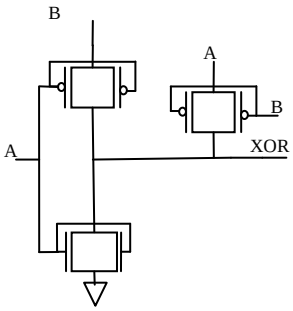


Fig.3(c)

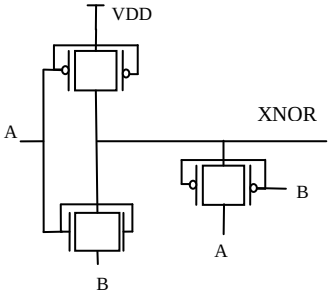


Fig. 3(d)

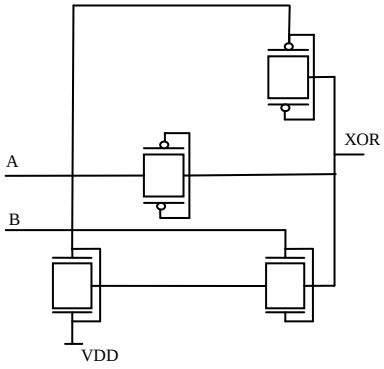


Fig. 3(e)

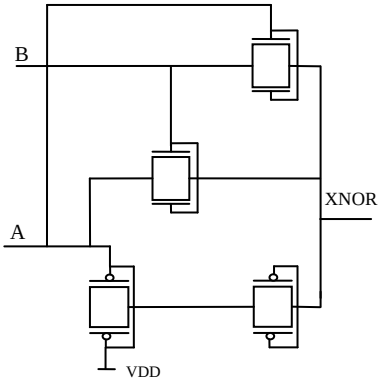


Fig. 3(f)

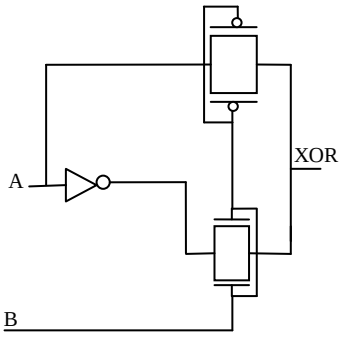


Fig. 3(g)

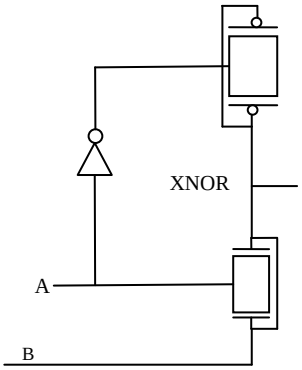


Fig. 3(h)

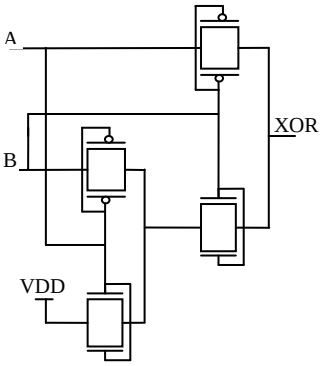


Fig. 3(i)

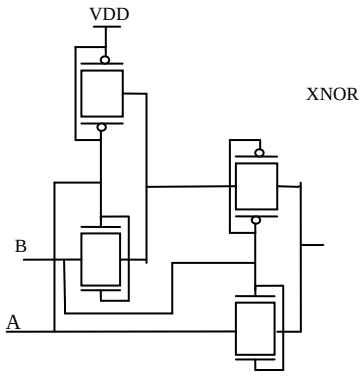


Fig.3 (j)

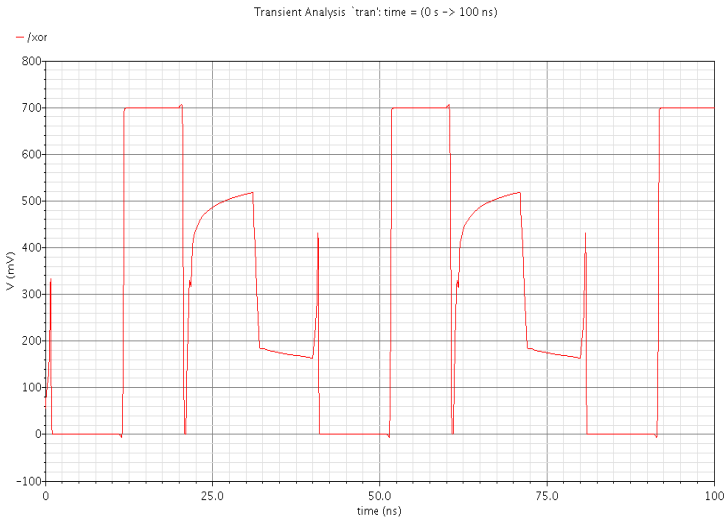


Fig. 3(k): *Output Waveform of Fig.3 (h)*

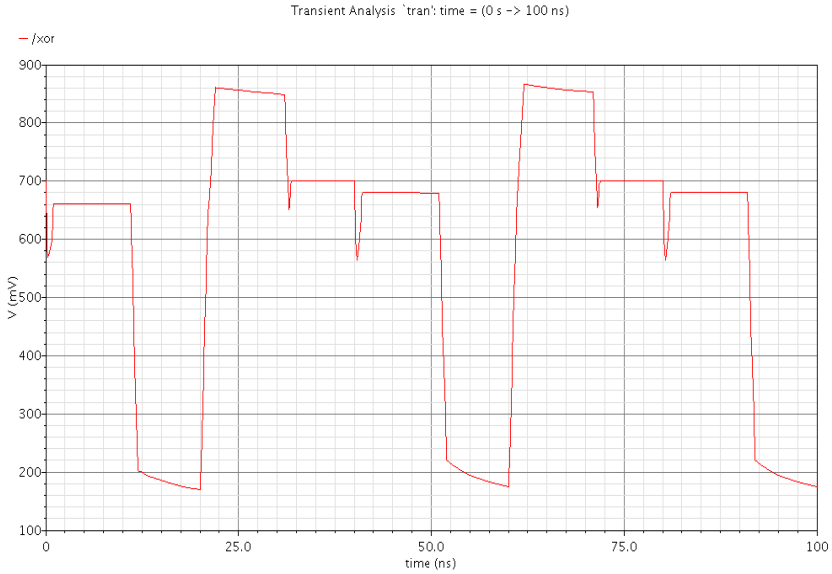


Fig. 3(l): *Output Waveform of Fig. 3(i)*

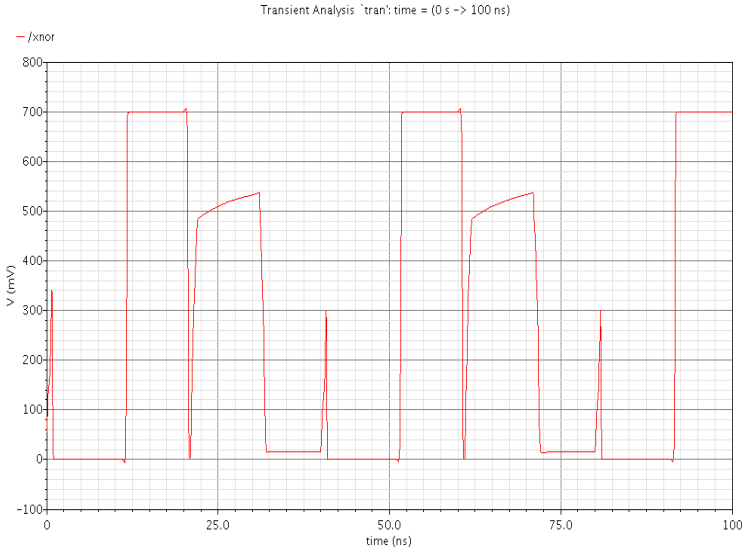


Fig. 3(m): *Output Waveform of*

When input is high (logic 1), the PMOS pass transistor is OFF and NMOS pass transistor is ON. When input B is high (logic 1), PMOS is OFF and NOMS is ON, therefore the output of XOR circuit in Figure 3 (a) is complement of input A i.e. (A'). In the Figure 3 (b), when input B is low (logic 0), the output of XNOR circuit is complement of input A i.e. (A'). In the Figure 3 (c), when input B is high (logic 1), inverter circuit functions like a normal inverter, therefore the output of XOR circuit is complement of input A i.e. (A'). When input B is low (logic 0), the output of inverter is at high impedance. Still the PMOS transistor is ON and output value becomes same as input A. It performs non full- swing operations for same inputs. Similarly output voltage degrades in respect to input voltage when A=0 and B=1 in Figure 3(d). Output voltage swings in XOR and XNOR circuits in Figure 3(e) and Figure 3(f) and reduces power consumption but driving capability is reduced due to the degraded output voltage.

XOR and XNOR circuits furnish good output levels in Figure 3(g) and Figure 3(h). Due to use of inverter in these circuits the repelling capability is also improved. Figure 3(i) and Figure 3(j) show a set of low power 3-transistors of XOR and XNOR circuits, which are called powerless XOR and groundless XNOR circuits. Figure 3(i) is similar to Figure 3(g), the sole difference is VDD connection in circuit. XOR and XNOR circuit in Figure 3(i) and (j) consume less power than other circuits designs because there is no power supply (VDD) and ground connection (VSS).

D. XOR and XNOR Circuits with Feedback Transistors

In multiplexer, control signal lines etc, selection lines are used, the combined XOR-XNOR cell can be used to drive the selection line. The concurrent generation of the two non-skewed outputs is highly desirable. To defeat the problem of the skewed outputs some designs that combine the execution of both XOR-XNOR functions in the circuit, are discussed below. This circuit is designed based on complementary input signals. In this methodology, the number of transistors increase but the performance is greatly enhanced. This methodology is the use of feedback transistors [22- 23].

The first circuit is shown in Figure 4(a) in these circuit two PMOS (pull-up) transistors P1 and P2 and two NMOS (pull-down) transistors N1 and N2 augment the basic skeleton. Furthermore, both the circuits immobile fail to provide good outputs level for one input vector. They bid "bad 0" output at XOR for input pattern "00". In the same way, for XNOR function, at input "01" produces a "bad 0". This can be corrected by the use of the two pull-down transistors N1 and N2 in the XNOR network. The output waveform of Figure 4(a) and 4(b) are shown in Figure 4(c), (d).

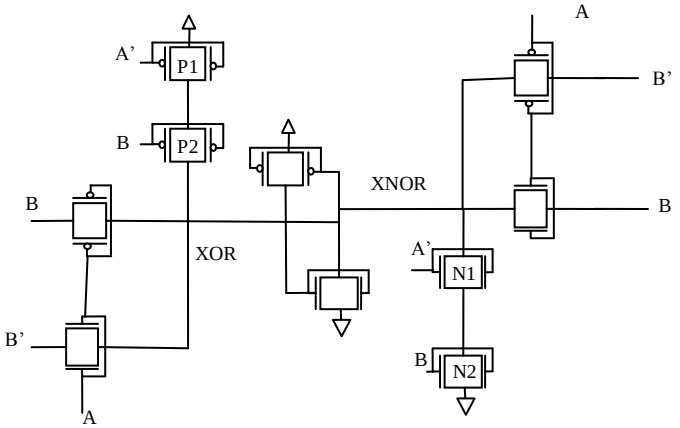


Fig. 4(a)

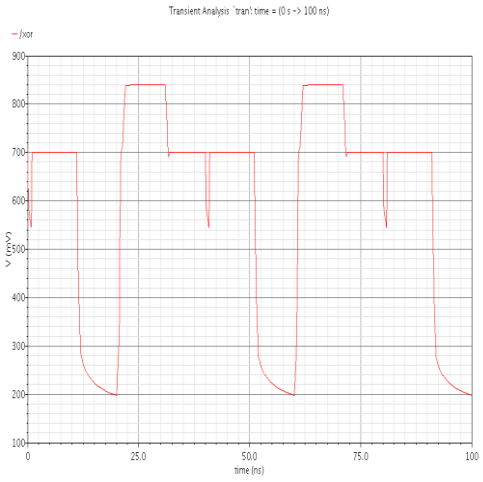


Fig. 4(c): Output Waveform of Fig.4(a).

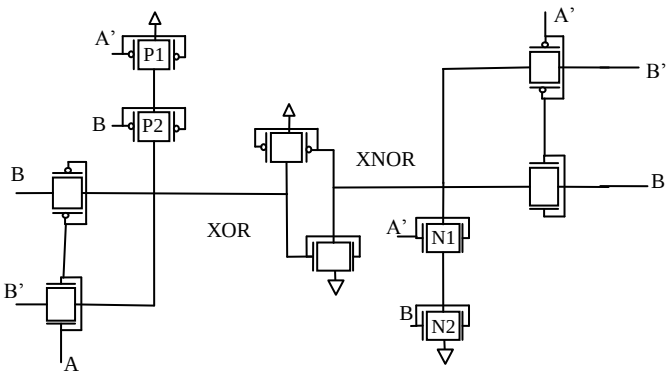


Fig. 4(b)

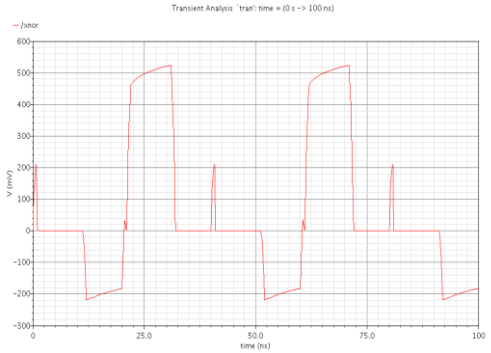


Fig. 4(d): *Output Waveform of Fig.4(b)*

Input and output values for the Fig.4

Input		Output	
A	***B***	***XOR***	***XNOR***
0	0	Bad 0	Good 1
0	1	Good 1	Bad 0
1	0	Bad 1	Good 0
1	1	Good 0	Bad 1

Input and output values for the Fig.5

Input		Output	
A	***B***	***XOR***	***XNOR***
0	0	Good 0	Good 1
0	1	Good 1	Good 0
1	0	Good 1	Good 0
1	1	Good 0	Good 1

The improved version of the above circuits is shown in Figure 5(a) and 5(b). The dual feedback network is used to correct the degraded logic level problem i.e. forward feedback loop is used to amend the output voltage level for input combinations (00) and (11) while feedback loop is used to improve the output logic level of the circuit for input combinations (01) and (10). This feedback configuration increases the circuit performance as well as fan out also.

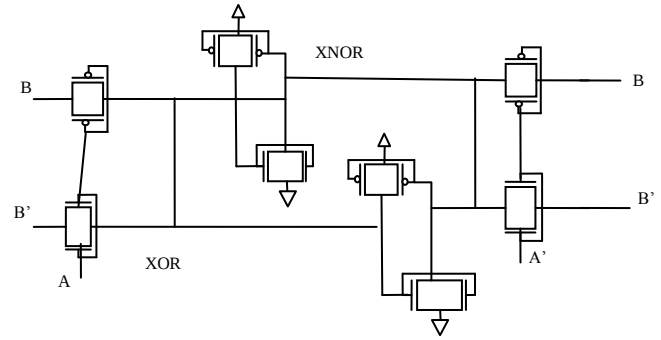


Fig. 5(a)

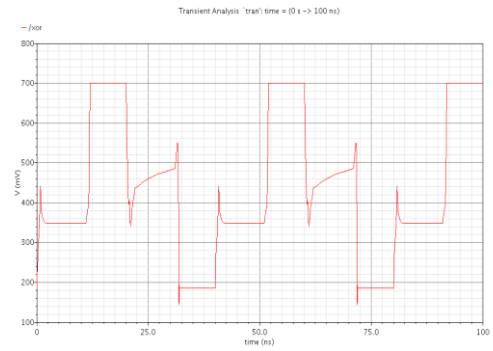


Fig. 5(c): Output Waveform of Fig. 5(a)

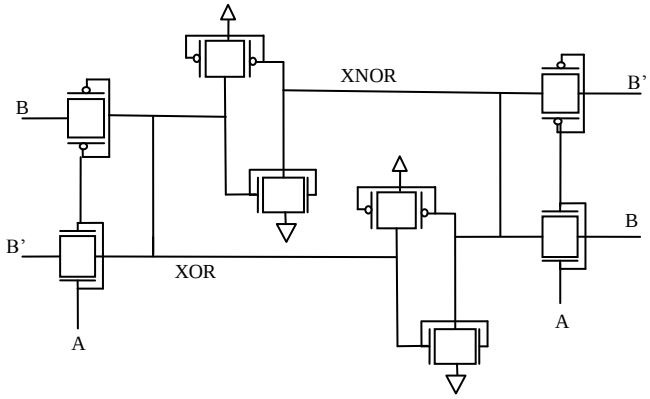


Fig. 5(b)

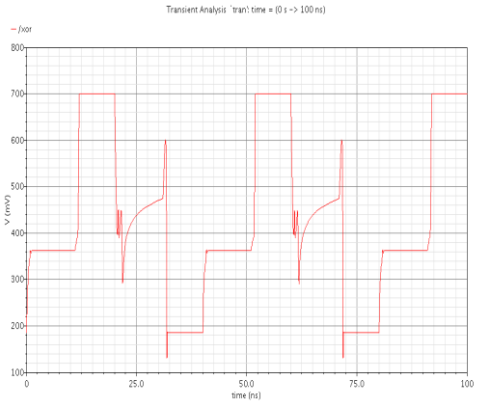


Fig. 5(d): *Output Waveform of Fig. 5(b)*

E. Transmission Gate Based Xor and Xnor Circuits

Transmission gate CMOS (TG) uses transmission gate logic to realize complex logic functions using a small number of complementary transistors. In Figure 6(a) shows 10-T circuit for XOR and XNOR function, this is based on transmission gates [23] and inverters. In this circuit design is composed of two transmission gate and three inverters. Because of its transmission gates it offers full swing output levels. Due to use of static inverters, its driving capability is also excellent. The output of XNOR is heavily tilted in the time from XOR output since XNOR is inverted to achieve XOR. The output waveform is shown in Figure 6(c).

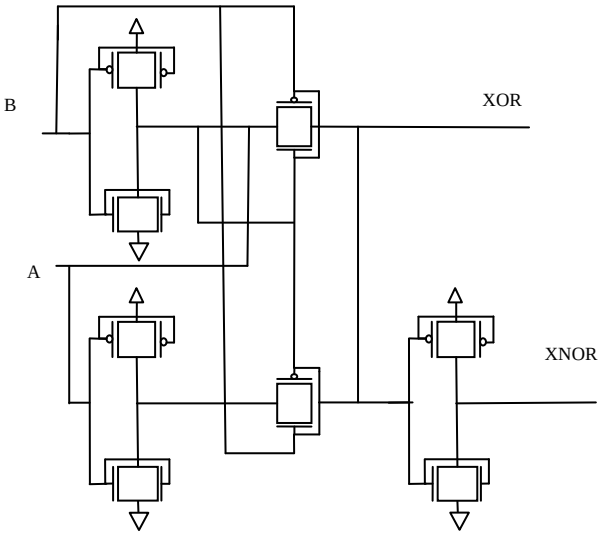


Fig. 6(a)

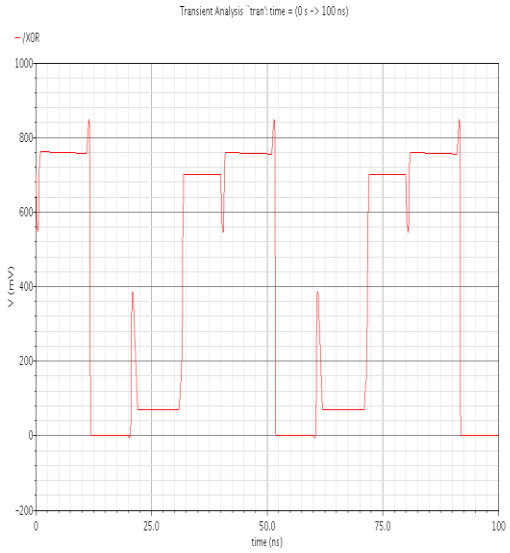


Fig. 6(c): *Output waveform of Fig. 6(a).*

Figure 6(b) shows an attractive XOR-XNOR circuit with 5 transistors [24] by generating XOR –XNOR outputs simultaneously, this circuit attempts to defeat the problem of skewed outputs. The connection between VDD and GND provide good driving capability to the circuit. It consumes higher dynamic power due to short circuit current for input transistors that leads to input vector "11" or "00". This occurs because, feedback transistors is switch on by weak signal and other signal at high impendence state. The XOR and XNOR signal remains moment in high impedance state for transition to the input vector "11" ("00"). The output waveform is shown in Figure 6(d).

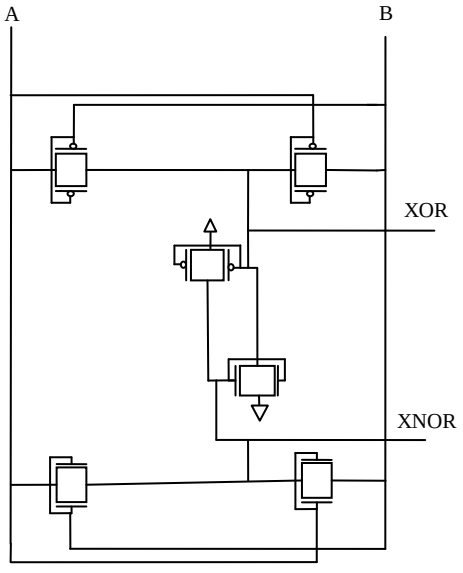


Fig. 6(b)

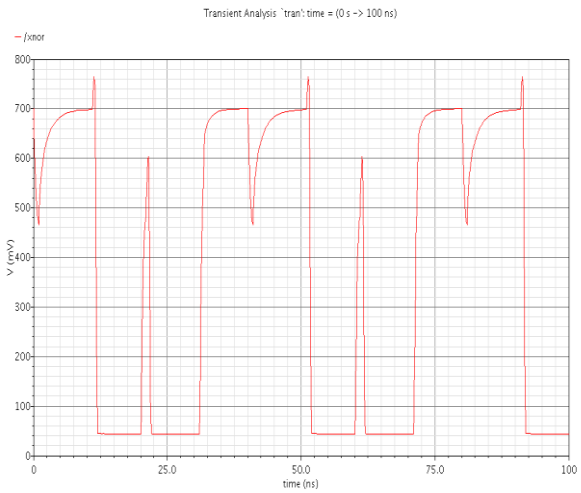


Fig. 6(d): *Output Waveform of Fig. 6(b).*

F.GDI based XOR and XNOR Circuit

Gate diffusion input (GDI) is based on the use of simple GDI input cell as shown in Figure 7, and GDI is a low power digital combinational design technique.

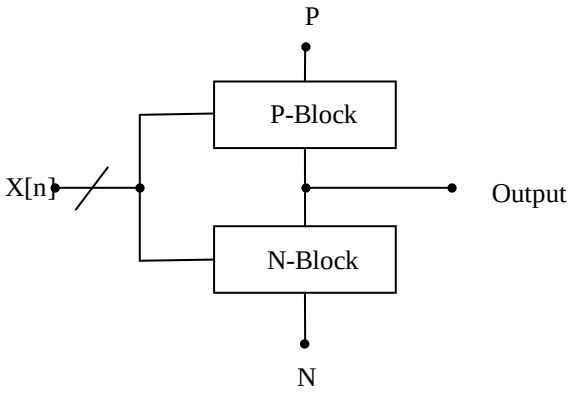


Fig 7(a): *(n + 2) Inputs Gdi Cell.*

The basic difference between standard CMOS inverter cell and GDI cell is as follow: The GDI cell has three inputs G (common gate input of transistors PMOS and NMOS), N (input to the source/drain of NMOS), and P (input to the source/drain of PMOS). Bulks of both PMOS and NMOS are connected to P and N (respectively), so it can be randomly biased at contrast with a CMOS inverter. The GDI technique grants decreasing propagation delay, power consumption and area of digital circuit while holding low complexity of the logic design. 3- Transistor using GDI cell [25] is shown in Figure 7(b).

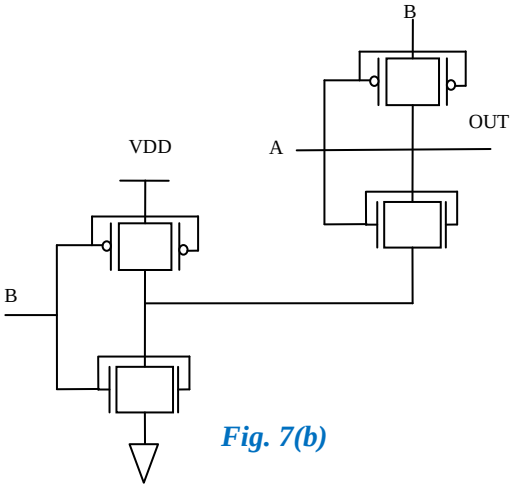


Fig. 7(b)

SIMULATION RESULTS

The transient and DC analysis of the circuits were generated by Cadence SPECTRE simulator in the voltage 0.6v at 34 nm technology. Simulation is performed at changing supply voltages to show the effect of different voltages to the power dissipation of XOR-XNOR circuit. The analysis has been carried out on the combination of XOR-XNOR, based on the previous design. The delay has been computed between the times when the changing input reaches 40% of voltage level to the time its output reaches 40% of voltage level for both rise and fall transition. The power-delay product (PDP) is measured as the product of the average delay and the average power. The energy delay product (EDP) is measured as the product of the average delay and power delay product. These results are compared with previous publish papers, which are shown in below Table 2.

Table 2: *Output Values for Fig.1(A) To 1(C).*

Performance Parameter	Fig. 1 (a)	[8]	Fig. 1(b)	[8]	Fig. 1(c)	[8]
Delay(s)	250.4E-12	0.046E-9	123.5E-12	0.86E-9	0.1092E-12	0.595E-9
Average dynamic power consumption(w)	1.368E-6	6.868-05	2.45E-6	6.443E-5	7.979E-9	7.7644E-5
Power delay product(J)	3.425E-10	3.1456E-15	3.025E-15	5.54E-15	8.713E-15	6.83E-15
Energy delay product (s*fJ)	0.8576	0.1447	0.373	0.465	0.9514	0.6013

Table 3: *Output Values for Fig.2(A) To 3(A).*

Performance Parameter	Fig. 2(a)	[8]	Fig. 2 (b)	[8]	Fig. 3(a)	[8]
Delay(s)	11.37E-9	0.0825E-9	12.16E-10	0.085E-9	11.29E-10	0.0415E-9
Average dynamic power consumption(w)	22.36E-9	6.5126E-5	23.27E-9	43.727E-5	164.5E-9	6.3513E-5
Power delay product(J)	2.542E-15	0.5373E-15	2.82E-15	3.7167E-15	1.857E-15	2.6357E-15
Energy delay product (s*fJ)	0.0288	.0443	0.0341	.3159	2.08	0.1094

Table 4: *Output Values for Fig.3(b) to 3(D).*

Performance parameters	Fig. 3(b)	[8]	Fig. 3(c)	[8]	Fig. 3(d)	[8]
Delay(ns)	11.17E-10	0.37E-9	375.6E-12	0.55E-9	121.1E-12	0.395E-9
Average dynamic power consumption(w)	9.327E-9	6.22E-5	1.896E-9	.3638E-5	1.741E-10	0.3408E-5
Power delay product(J)	0.104E-15	0.2301E-15	0.7121E-15	2.0009E-15	0.0208E-15	0.134E-15
Energy delay product (s*fJ)	0.0011	0.0085	0.026	0.11	0.0025	0.0005

Table 5: *Output Values for Fig.3(E) to 3(g).*

Performance parameters	Fig. 3(b)	[8]	Fig. 3(c)	[8]	Fig. 3(d)	[8]
Delay(ns)	11.17E-10	0.37E-9	375.6E-12	0.55E-9	121.1E-12	0.395E-9
Average dynamic power consumption(w)	9.327E-9	6.22E-5	1.896E-9	.3638E-5	1.741E-10	0.3408E-5
Power delay product(J)	0.104E-15	0.2301E-15	0.7121E-15	2.0009E-15	0.0208E-15	0.134E-15
Energy delay product (s*fJ)	0.0011	0.0085	0.026	0.11	0.0025	0.0005

Table 6: *Output Values for Fig.3(H) to 3(J).*

Performance parameters	Fig. 3(h)	[8]	Fig. 3(i)	[8]	Fig. 3(j)	[8]
Delay(ns)	11.7E-12	0.44E-9	11.15E-12	0.231E-9	11.18E-12	0.422E-9
Average dynamic power consumption(w)	9.327E-9	1.1338E-5	299.1E-12	2.5872E-5	5.975E-9	3.3912E-5
Power delay product(J)	0.109E-15	0.4988E-15	3.33E-15	5.9764E-15	1.668E-15	1.4311E-15
Energy delay product (s*fJ)	0.127	0.2195	0.374	1.3805	0.0741	.06039

Table 7: *Output Values for Fig.4(A) to 5(a).*

Performance parameters	Fig. 4(a)	[8]	Fig. 4(b)	[8]	Fig. 5(a)	[8]
Delay(ns)	8.89E-10	0.1570E-9	21.12E-10	0.1325E-6	106.5E-12	0.1155E-9
Average dynamic power consumption(w)	4.92E-9	13.43E-5	8.87E-6	9.78E-5	768.67E-9	16.47E-5
Power delay product(J)	4.38E-15	21.286E-15	1.88E-15	12.958E-15	8.19E-15	19.02E-15
Energy delay product (s*fJ)	2.8	3.373	1.39	1.717	1.864	2.197

Table 8: *Output Values for Fig.5(b) to 7(b).*

Performance parameters	Fig. 5(b)	[8]	Fig. 6(a)	[9]	Fig. 6(b)	[9]	Fig. 7(b)
Delay(ns)	11.67E-12	0.1295E-9	11.0E-9	2.501E-8	148.2E-12	3.440E-9	21.0E-9
Average dynamic power consumption(w)	762.3E-9	20.13E-5	23.69E-6	-	1.65E-6	-	32.3E-6
Power delay product(J)	8.89E-15	26.068E-15	9.42E-15	-	2.45E-15	-	6.76E-15
Energy delay product (s*fJ)	1.02	3.3758	1.03	6.596	3.63	1.036	1.42

CONCLUSION

In this paper, various FinFET based XOR/XNOR circuits have been designed and analyzed. The referred design techniques are compared based on a delay, power delay product (PDP), average dynamic power consumption. The performances of these techniques have been calculated by cadence using virtuoso tool at 34 nm technology. Various parameters such as delay, power delay product (PDP), average dynamic power consumption have been calculated. These designs are suitable for various VLSI applications and arithmetic circuits. Based on simulation results, it has been culminated that the PTL based XOR and XNOR circuits outputs high (or low) voltage are varied from the VDD (or ground). It is concluded that Figure 3(i), Figure 3(j), 4(a) to 6(b) have reduced delay, power consumption, reduced power delay product and consume less area.

ACKNOWLEDGMENT

The Endeavour in this paper was supported by ITM University, Gwalior, India with the collaboration of Cadence System Design, Bangalore, India.

REFERENCES

1. Subodh Wairya, Rajendra Kumar Nagaria, Sudarshan Tiwari. Comparative Performance Analysis of XOR-XNOR

Function Based High-Speed CMOS Full Adder Circuits For Low Voltage VLSI Design. *International Journal of VLSI Design & Communication Systems (VLSICS)*. 2012; 3(2).

2. Feng Wang, Yuan Xie, Kerry Bernstein, et al. Dependability Analysis of Nano-Scale FinFET Circuits. *Proceedings of the 2005 Emerging VLSI Technologies and Architectures (ISVLSI'05) 0-6594-2433-3/05*.
3. Seid Hadi Rasouli, Hanpei Koike, Kaustav Banerjee. High-Speed Low-Power FinFET Based Domino Logic. *IEEE Conference on Design Automatoion Conference*. 2009; 729–733p.
4. Hisamoto, D., et al. Finfet-A Self-Aligned Double-Gate Mosfet Scalable To 20 nm. *IEEE Trans. Electron Devices*. 2000; 2320– 2324p.
5. Michael C. Wang. An Overview of Independent-Gate FinFET Circuit Synthesis. *IAENG Transactions on Engineering Technologies*. 2010; 3.
6. Sherif A. Tawfik, Volkan Kursun. Low-Power and Compact Sequential Circuits With Independent-Gate FinFETs. *Ieee Transactions on Electron Devices*. 2007; 44(1).
7. Animesh Datta, Ashish Goel, Riza Tamer Cakici,et al. Modeling and Circuit Synthesis for Independently Controlled Double Gate FinFET Devices. *IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems*. 2006; 25(11).
8. Shiv Shankar Mishra, Adarsh Kumar Agrawal, R.K. Nagaria. A Comparative Performance Analysis of Various Cmos Design Techniques for Xor and Xnor Circuits. *International Journal on Emerging Technologies*. 2010;1(1): 1–10p.
9. Aminul Islam A. Imran, Mohd. Hasan. Variability Analysis and FinFET-Based Design of XOR and XNOR Circuit. *International Conference on Computer & Communication Technology (ICCCT)*. 2011; 239– 234p.
10. Nabihah Ahmadm, Rezaul Hasan. A New Design of Xor-Xnor Gates for Low Power Application. *2011 International Conference on Electronic Devices, Systems & Applications (ICEDSA)*.
11. N. Weste, K. Eshranghian. Principles of CMOS VLSI Design: A System Perspective, Reading MA: Addison-Wesley. 1993.
12. Sung-Mo Kang, Y. Leblibici. CMOS Digital Integrated Circuits: Analysis and Design, Addition-Tata McGraw Hill. 2003.
13. J.Rabaey. Digital Integrated Circuits (A Design Prospective), Prentice-Hall, Englewood Cliffs, NJ. 1995.
14. H. Lee, G. E. Sobelman. New Low-Voltage Circuits For Xor and Xnor. *In Proc. IEEE Southeastcon*. 1996; 224–229p.
15. R. Zimmermann, W. Fichtner. Low-Power Logic Styles: Cmos Versus Pass-Transistor Logic. *IEEE J. Solid-State Circuits*. 1996; 32(6): 1069–1090p.
16. K. Yano et al. Top-Down Pass-Transistor Logic Design. *IEEE J. Solid-State Circuits*. 1995; 31(5): 692–703p.
17. Lara D. Oliver, Krishnendu Chakrabarty, Hisham Z. Massoud. Dual-Threshold Pass-Transistor Logic Design. 2009; 291–295p.
18. Chiraz Khedhiri, Mouna Karmani, Belgacem Hamdi. A Differential Double Pass Transistor Logic Unit. *IJCSI International Journal of Computer Science Issues*. 2012; 9(2) 341-343p.
19. K. Yano, T. Yamanaka, T. Nishida, et al. A 3.7 Ns Cmos 15 * 15 Multiplier Using Complementary Pass-Gate Transistor Logic. *IEEE J. Solid-Sate Circuits*. 1990; 24: 377–394p.
20. M. Suzuki et. al. A 1.4 Ns 32-Bit Cmos Alu in Double Pass-Transistor Logic. *In Proc. IEEE Int. Solid-State Circuits Conf*. 1993; 35: 90–91.
21. V.G. Oklobdz˘ija, B. Duchene. Pass-Transistor Dual Value Logic for Low-Power CMOS. *Proceedings of the 1994 International Symposium on VLSI Technology, Systems, and Applications*. 1994; 331–333p.
22. Sumeer Goel, Mohammed A Elgamel, MA Bayoumi. Design Methodologies for High-Performance Noise- Tolerant XOR-XNOR Circuits. *IEEE Trans. Circuits Syst. I*. 2005; 43(3).

23. Sumeer Goel, Mohammed A Elgamel, MA Bayoumi. Novel Design Methodology for High-Performance Xor– Xnor Circuit Design. *In Proc. 15th Symp. Integr. Circuits Syst. Design.* 2003; 61–65p.
24. A.M. Sharms, T.K. Darwish, M.A. Bayoumi. Performance Analysis of Low-Power 1-Bit Cmos Full Adder Cells. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* 2002; 10(1): 20–29p.
25. D. Radhakrishanan. Low-Voltage Low-Power Cmos Full Adder. *In Proc. IEE Circuits Devices Syst*. 2001; 137.