A Survey of Wideband Low Noise Amplifiers Design Techniques for Cognitive Radios

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Abstract— this paper surveys recent research on Low Noise Amplifier (LNA) design for Cognitive Radios (CR). Design challenges and requirements of CR are discussed and recent advances in topologies and design techniques are presented, compared and summarized. The classical trade-offs of linearity, gain, input impedance matching and noise are discussed herein with respect to the Wide Bandwidth requirement.

Keywords— LNA Design, Low Noise Amplifier, Wideband, RF, Cognitive Radio.

I. INTRODUCTION

The growth of mobile devices popularity has made wireless communications a hot subject on research around the world. The Software Defined Radio (SDR) concept was initially used as a solution to the increasingly demand for multi-band, multi-standard radios, proposing multiple software-programmable radios to accomplish the multi-standard need. However, the utilization of multi-narrowband radios consumed too much area and power.

The wideband Low Noise Amplifier (LNA) concept has attracted attention since SDRs became popular. The idea was to save area and power on a multi-standard device.

As the cellular and wireless LAN frequency spectra approach its occupation limits, the concept of Cognitive Radio (CR) has been proposed as a solution to improve spectrum utilization efficiency. An intelligent radio capable of deciding for itself to change its frequency band based on spectrum activity monitoring is the essence of CR \cite{1-2}. The implementation of CR was first intended to be used in the TV Broadcast band, which became available after migration to Digital TV (DTV). The extension of CR concept to cellular and WLAN spectra is expected as a future technology to help solving frequency spectrum congestion problems.

The challenges in designing CR are more difficult than SDR \cite{3}. Unlike SDR, CR does not target certain standards and their allocation bands and must operate at any frequency in the specified range. While SDR has previous information about used and unused channels and band, CR must sense and detect unoccupied channels, which might be a difficult and slow task.

Based on this scenario, the wideband LNAs used in SDR might not be suitable for CR mainly to the linearity constraints \cite{4}. In a dynamic allocated spectrum, the linearity requirement is a critical issue. In such a wideband, the LNA can mix unwanted signal back to its operating frequency band due to its own nonlinearity, increasing the mixer requirements and degrading the overall signal-to-noise ratio (SNR) of the receiver.

In this work, a survey on recent published works about wideband LNAs for CR and theirs implementation techniques is presented. The feedback technique improves input matching, which improves Noise Figure (NF), while contributing in linearization. Noise cancelling can be used along with feedback to reduce NF by subtracting inverted correlated noise signals \cite{5-10}. Other linearization method is based on cancelling higher order nonlinear terms of the signal of interest by adding a secondary device to subtract currents or voltages \cite{11-12}. The key idea is to improve the linearity of a wideband LNA (previously targeting SDR) without degrading gain, NF and input impedance matching, and working in a 2-3 decades frequency bandwidth.

This paper is organized as follows: in section II the feedback and noise-cancelling Wideband LNAs (WBLNAs) are discussed, in section III WBLNAs using linearization techniques are analyzed, in section IV the advantages and disadvantages of each strategy are presented and the conclusions are in section V.

II. THE FEEDBACK AND NOISE-CANCELLING WBLNA

The shunt-feedback technique showed in figure 1 is perhaps the simplest way of reducing the LNA noise figure. It works by scaling its input impedance to match properly the low source impedance. But in this strategy, the input impedance Zin relies directly on the LNA gain. Also, a variable gain (depending on the process) directly degrades the impedance matching. Not to mention the instability issue due to cascaded stages used to achieve high gain in deep sub-micron technologies.

A better strategy is to break this direct connection of Zin, NF and gain, keeping the feedback advantages. In \cite{10}, the feedback problems and the noise cancelling technique are well
described and explained. The implementation was made in CMOS 250 nm. Figure 2 shows the noise cancelling technique for a single-ended amplifier. The idea behind noise cancelation is the addition of another amplifier, which inverts the LNA input signal and noise, generating an output signal that can be added to the direct path signal to subtract noise and enhance gain.

Figure 1: Negative Feedback Common-Source.

One possible problem of this technique is the noise generated by the added amplifier. However, the noise generated from this amplifier is completely decoupled from the noise of the direct LNA. Thus, it can achieve very low values of NF without degrading input impedance and LNA total gain. Besides, even with mismatch problems, which can shift noise and signal phases, noise is still partially cancelled. This technique can achieve a NF below 2.5 in the entire band.

Figure 2: Feedback + Noise Cancellation Concept [10].

The work in [9] uses the feedback + noise cancellation concept to implement a differential WBLNA in CMOS 130 nm process (Figure 3). It incorporates the differential advantages, such as improved noise cancellation (common mode rejection) and enhanced gain to accomplish the challenge of implementing the idea in CMOS 130 nm and shows a NF around 3-5 dB.

In [8], the feedback noise cancelling was implemented in a different way. It included the additional cancelling amplifier within a cascode WBLNA (figure 4). The cancellation occurs in the Vgs of the common-gate stage. This design also enhances gain and contributes to achieve a total receiver NF of 3 dB. The implementation of the G amplifier of Figure 4 was simply a short-circuit (G=1).

In [7], a Common Gate (CG) differential amplifier was used along with a Common Source (CS) to implement noise cancellation without resistive feedback. Figure 5 shows the implementation, which achieved 1.4-2.5 dB NF.

Figure 3: Differential WBLNA using feedback + noise cancelling technique in 130 nm [9].

Figure 4: Differential Cascode feedback + noise cancelling technique in 130 nm [8].

Figure 5: Differential WBLNA using noise cancellation without resistive feedback [7].

The input signal enters the common-gate and common-source amplifiers, and then both output signals with different polarities are summed to cancel noise.

Apart from differential implementations, single-ended (such as in [10]) might be needed, depending on the antenna and RF filter used on the WBLNA input. In [6], a single-ended WBLNA was implemented in CMOS 90 nm. It uses the same idea of [7], i.e., CG + CS amplifiers for noise cancellation. However, it uses resistive and inductive
degeneration to achieve NF as low as 2.3 dB in 90 nm. The circuit is shown in Figure 6.

![Figure 6: Noise cancellation with inductive and resistive degeneration][6]

The work in [5] uses the same 3 cascaded CS stages with differential output of [4], but with source RC degeneration in the last CS stage, improving matching between the noise cancelling nodes and linearity at the same time. Source degeneration is applied (RC parallel branch) in the third stage to lower the gain, as well as providing better matching between nodes X and Y, besides improving also the linearity. However, the source degeneration resistor Rdeg degrades the high frequency input matching. Thus, the degeneration capacitor Cdeg is added to boost up the bandwidth of the balun-LNA, helping as well the input impedance matching at high frequency. The circuit of [5] is showed in Figure 7. It achieves 2.7-3.6 dB NF in 65 nm.

![Figure 7: Cascaded CS stages with differential output and source degeneration][5]

All of the above topologies improved NF of WBLNAs while maintaining gain and input impedance matching. As noise cancellation also cancels high order harmonics, linearity is also improved. However, this improvement might not be enough for CR applications, though, needing more linearity improvement. The linearity improved WBLNAs are discussed in the following section.

### III. Linearization Techniques for WBLNA

The feedback + noise cancellation technique achieves IIP3 around 0 dBm. This is because its main purpose is to cancel noise without degrading input impedance matching and gain.

In CR, however, higher IIP3 values might be required, regarding its wide bandwidth. In order to solve this linearity problem, some new techniques have been developed. A great result is achieved in [11], where the cascode CG WBLNA has its IIP3 improved by +11.7 to +14.1 dBm, without degrading gain and NF in CMOS 130 nm. The circuit is shown in Figure 8.

![Figure 8: Cascode CG WBLNA using linearization technique][11]

The CG stage is used to improve input impedance matching and the cascode is used to improve gain and bandwidth. The inductor Ld increases bandwidth and inductor Lc cancels parasitic effects of the cascode transistors. The amplifier at the right of the design is a buffer, used to interface the measurement equipment and also emulates the input impedance of a mixer. The key component of this design is the diode-connected transistor at the drain of the CG input stage. This transistor taps the drain voltage, replicating the CG current. The output current which goes to the cascode transistor is the subtraction of both currents, partially cancelling second and third order nonlinear terms. Although this technique also cancels the linear term, it does not degrade gain/NF because the diode bias is much less than that of the CG transistor. The complete analysis of the nonlinearity of this topology is showed in [11] with Volterra series expansion. The linearization technique is designed for 1.5 GHz to 8.1 GHz.

The above linearity analysis considered the CG input transistor nonlinearity as dominant, neglecting the output conductance and cascode transistor nonlinearities. This approach is well suited to long channel devices and high supply voltages. In deep-submicron technologies, the output resistance is typically low, increasing the distortion of the cascode transistor. Besides, the low voltage operation might
push the cascode transistor out of deep saturation, which also increases the distortion of the circuit.

The work in [12] makes a rigorous analysis of the differential resistive feedback cascode WBLNA, considering the transconductor, output resistance and cascode transistor nonlinearities. A method of intermodulation-product of third-order (IM3) cancellation is proposed using negative impedance connected in the middle of the cascode, as shown in Figure 9. The 4 transistors plus the capacitor in the middle implements the negative impedance.

![Figure 9: Negative impedance linearization technique implemented on Differential resistive feedback cascode WBLNA [12].](image)

The idea of the negative impedance is to generate a degree of freedom in cancelling the nonlinear terms of all the components considered. The nonlinearity symbolic analysis was made based on harmonic balance to arrive at a given expression for the current of the cascode in terms of vgs, vds and the negative impedance added. The exact expression was not imported, what matters is the required value on the negative impedance to partially or fully cancel the IM3 contributions of both the cascode transistors. The thermal noise addition of the negative impedance does not degrade the performance, since the noises of all the other components are lowered by the negative impedance effect. This topology without inductors achieves IIP3 improvements of 6.3 dB to 10 dB in 0.1 GHz to 1 GHz, while maintaining low NF, high gain and input impedance matching (using feedback).

### TABLE 1: Topologies parameters comparison

<table>
<thead>
<tr>
<th>Tech</th>
<th>BW(GHz)</th>
<th>Gain(dB)</th>
<th>NF(dB)</th>
<th>IIP3(dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>65nm</td>
<td>0.05-10</td>
<td>24-25</td>
<td>2.7-3.6</td>
<td>-10/-2</td>
</tr>
<tr>
<td>90nm</td>
<td>0.05-10</td>
<td>13.4-10.6</td>
<td>2.3-2.8</td>
<td>-5</td>
</tr>
<tr>
<td>130nm</td>
<td>0.05-5</td>
<td>12</td>
<td>1.4-2.4</td>
<td>-7.89</td>
</tr>
<tr>
<td>130nm</td>
<td>0.6-3</td>
<td>48.42</td>
<td>3</td>
<td>-14</td>
</tr>
<tr>
<td>130nm</td>
<td>0.5-1</td>
<td>11.12</td>
<td>3-5</td>
<td>0.72</td>
</tr>
<tr>
<td>130nm</td>
<td>0.2-1.6</td>
<td>13.7</td>
<td>2.4</td>
<td>0.72</td>
</tr>
<tr>
<td>130nm</td>
<td>0.8-8.4</td>
<td>9.6-12.6</td>
<td>3.3-5.5</td>
<td>3.9-8.5</td>
</tr>
<tr>
<td>160nm</td>
<td>0.1-1</td>
<td>12-17</td>
<td>4.5</td>
<td>1-11</td>
</tr>
</tbody>
</table>

*Entity receiver.

**IV. TOPOLOGIES COMPARISON**

Table 1 shows the parameters of the designs discussed in this paper. The reader can compare each of them to the adequate use needed.

The noise cancellation topologies are well suited for the sensing technique of CR, since linearity might be relaxed depending on the digital algorithm used after the front-end. The solution proposed in [5], without inductors, might be the smallest circuit and the best performance (depending on the implementation of the differential amplifier). The linearized WBLNAs are suited to any CR application, such as signal reception, since its linearity is at best currently encountered in the open literature. The work in [12], without inductors, is the smallest circuit to achieve high gain and high linearity above 0 dBm.

**V. CONCLUSIONS**

A survey on WBLNAs for CRs was presented, pointing the key details of recent topologies in the literature. The comparison showed the feedback noise cancelling technique can be used in a ultra-wideband CR. The linearized topologies accomplished the best results for linearity, being best suited to CR general applications. Our next goal is to contribute to a UFRGS design of a CR front-end in 130 nm CMOS.

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**REFERENCES**


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