ABSTRACT

High density compound materials (CdTe, GaAs, HgI2) are currently evaluated as direct photon conversion sensors for applications in X-ray imaging. A new front-end stage has been designed with the aim to be implemented as readout chain in a luggage inspection system based on a linear array of CdTe sensors. Both types of electron or hole collecting CdTe sensors will be evaluated. Each detecting element is characterized by leakage current smaller than 5nA/mm² at working point and capacitance in the range of 0.5pF. A low noise front-end chain has been developed based on the voltage mode architecture. The operation of the front-end stage is optimized for a 2pF capacitance, system input capacitance, and for energy range of 20-220keV. A prototype ASIC has been fabricated in a commercial 0.6um CMOS process.

1. INTRODUCTION

The readout architectures for radiation sensors can be divided in two major categories: the voltage mode architecture and the current mode architecture. In the current domain approach, the first stage after the detector is a transimpedance amplifier which conveys the current and then converts it to voltage. When high counting rates are required the use of current mode architecture is preferable [1-2]. In the voltage mode architecture, the signal is processed in the voltage domain and the first stage is a charge amplifier followed by a shaper. This is a widely adopted solution for multichannel VLSI readout electronics in many different fields such as High Energy Physics, medicine and material science. In X-ray imaging applications in particular, where noise performance is of primary concern, the use of voltage mode architecture is the best solution.

Fig. 1 shows the block diagram of a single channel of the front-end electronics. The first stage after the detector is a low noise charge amplifier. In order to provide the ASIC with the ability to process signals of both polarities (electrons or holes collecting sensors), a polarity select circuit is added after the charge amplifier. This makes the read out system suitable for both polarities. The next stage is a semi-Gaussian shaper which optimizes the noise performance of the system. A voltage amplifier is connected after the shaper to further amplify the signal. The final stage of the analog part of the read out system is a voltage discriminator which produces digital pulses fed to the counters. In order to set the discriminator thresholds, a 4-bit DAC per channel has been also implemented within the ASIC.

2. CdTe SENSORS FOR X-RAY LUGGAGE INSPECTION SYSTEM

Current X-ray luggage inspection systems are working with a combination of photodiode arrays followed by scintillator-photodiode arrays. The first layer of photodiodes records the low energy photons emitted by the X-ray generator. For energies over 20keV the detection efficiency of Si drops dramatically. In order to record photons with higher energies, scintillators serve as intermediate devices for X-ray to light conversion. A system based on a direct photon conversion array of sensors would present advantages in terms of linearity, uniformity and resolution. CdTe and CdZnTe sensors are regarded as promising devices for hard X-ray and γ-ray recording [3-4]. The high atomic number of the materials gives high detection efficiency relative to Si. A 2mm CdTe sensor keeps detection efficiency over 50% all the way up to 150 keV. The large band gap energy (1.44 for CdTe, 1.6 for CdZnTe) allows operation of the sensors at room temperatures. Due to low mobility and short life time of holes, in combination with losses due to trapping centers such as dislocations and defects, electron collection mode is preferable in CdTe detector systems. The short propagation length of holes in combination with charge accumulation phenomena, known as polarization effect, in the bulk of the material limits the use of CdTe sensors in high quality spectroscopic application. CdTe sensors are suitable for counting mode applications as luggage inspection systems.

Linear arrays of CdTe sensors are under evaluation as detecting elements for a luggage inspection system. A 20mm x 2mm x 2mm CdTe rod is lithographically patterned on one side in 20 pads measuring 0.9mm x 1.8mm and separated with a gap of 0.1mm. The pads and the entire backside are plated with Pt in order to form ohmic contacts. This way, 20 individual detecting elements with a common backside are formed. Thirty arrays of this type will be placed on a line in order to form a 60 cm long linear system for luggage inspection. Each sensor pad will be routed to the input of an electronics readout chain as depicted in Fig.1. Typical nominal working voltage of the sensors is 100 volts. A good uniformity of leakage currents with values around 5 nA is measured for each pad at 22 °C at 100 volts. The capacitance of each pad is below 1pF. With a careful interconnection design, to avoid parasitic effects, a total capacitance smaller than 2 pf can be reached at the input of each readout channel.
3. CIRCUIT DESCRIPTION

3.1 Charge amplifier

Fig. 2 shows the complete schematic of the charge amplifier. The single-ended folded cascode configuration is used due to the high gain, broad bandwidth and good stability that exhibits. The noise level of the preamplifier depends mainly on its input stage so the input device is the most important in the whole design [5-7]. A PMOS transistor has been chosen as input device because it gives lower flicker noise compared to an NMOS. In order to optimize the noise behavior, the input PMOS transistor is matched with the detector capacitance [5].

The feedback consists of a capacitor \( C_f \) in parallel with a resistance \( R_f \), which is implemented by a PMOS transistor operating in the linear region. The series of current pulses released by the detector are integrated on the feedback capacitance of the charge amplifier producing at its output voltage steps of approximately \( \frac{Q}{C_f} \), where \( Q \) is the total charge resulting from integrating the pulse. The feedback capacitor is discharged by the feedback resistance and the decay time is externally controlled through the bias voltage \( V_{\text{preamp}} \). The preamplifier is biased at the center of its operating range in order to accept input charge pulses of both polarities.

![Figure 2. Complete schematic of the charge amplifier.](image)

3.2 Polarity select circuit

The second stage of the front-end chain is a polarity select circuit which is shown in Fig. 3. It consists of the polarity amplifier, which is a typical two-stage amplifier with high gain and broad bandwidth, four switches and two identical resistors. All the switches are implemented with PMOS devices and are controlled externally by the same signal. When the control signal \( PS \) is high the switches SW1 and SW2 turn off while the SW3 and SW4 turn on. In that case the gain of the polarity select circuit is \( A_{\text{pol}} = 1 \) and practically operates like a buffer. When the control signal \( PS \) is low the gain of the stage is \( A_{\text{pol}} = -1 \), as \( R_{p1} = R_{p2} \), and the polarity circuit inverts its input signal. In this way at the output of the polarity select circuit the voltage steps have the same polarity regardless the polarity of the input pulses, which can be either positive or negative. So the same front-end chain can be used to process signals produced either from electron collecting sensors or from hole collecting sensors.

![Figure 3. Block diagram of the polarity select circuit.](image)

3.3 Shaper

The stage following the polarity select circuit is the shaper which is a filter that optimizes the noise behavior of the system. As in the charge amplifier circuit, the single-ended folded cascode configuration is used with a PMOS as an input device. It is...
shown that when increasing the order of the filter only small improvement in noise performance is achieved [5]. Keeping that in mind and in order to have simpler circuit, the order of the shaper is set to 1. In the frequency domain, the shaper acts as a band-pass filter limiting the noise produced by the preamplifier and thus increasing the signal to noise ratio (S/N). In time domain, the voltage steps produced by the preamplifier are converted into semi-Gaussian output pulses. The shaping time is determined by the values of the capacitors, $C_{cs}$, $C_{fs}$ and $C_{hs}$, and the feedback resistance $R_{fs}$, which is implemented by a PMOS transistor. The optimum shaping time is calculated in order to optimize the noise of the system taking also into account the noise of the preamplifier. It is possible to adjust the shaping time through the gate voltage of the PMOS transistor connected in the feedback.

3.4 Voltage Amplifier

In many cases, apart from the gain achieved by the preamplifier and the shaper, a further amplification is needed so a voltage amplifier is also added. The amplifier is a two stage compensated Miller opamp with high open loop gain and good driving capability. The closed loop gain of the preamplifier is set to $A_{amp} = -2$.

3.5 Discriminator

The final stage of the analog part of the front-end is the discriminator. Fig. 4 shows the complete schematic of the discriminator. The output of the voltage amplifier is AC coupled to the input of the discriminator. This way, the DC level in the input of the discriminator is externally controlled. The discriminator circuit consists of three stages. The first stage is a simple source follower which significantly reduces the load of the voltage amplifier. The second stage, which is the core of the discriminator, is a high gain differential amplifier. Hysteresis is achieved by adding two cross-coupled PMOS devices. Finally, two CMOS inverters are connected to improve the shape of the output pulse. The threshold of the discriminator is fine adjusted through a 4-bit DAC cell which is implemented within the ASIC.

Figure 4. Complete schematic of the discriminator.

4. SIMULATION RESULTS

The front-end electronics have been designed in a 0.6um CMOS process with 3.3V power supply. Fig. 5 depicts the response at the output of the voltage amplifier for three different values of input charges, namely 1fC, 4fC and 8fC. The total gain of the chain is 130mV/fC while the peaking time is 35ns. The front-end stage recovers to the baseline within 400ns. The linearity of the chain is excellent up to 8fC, which corresponds to 220keV. The voltage pulses produced at the output of the discriminator in the case of 4fC input charge and event rate of 2Mevents/s is shown in Fig. 6. These pulses are subsequently fed to the digital part of the system for counting.

Figure 5. Transient response at the output of the voltage amplifier (input charge 1, 4, 8fC).

Figure 6. Voltage pulses produced at the output of the discriminator (input charge 4fC, event rate 2Mevents/s).

5. EXPERIMENTAL RESULTS

Fig. 7 shows the microphotograph of the fabricated ASIC. On the left of the chip is the analog part of each channel while on the right the mixed analog-digital part. Special layout techniques, including different power supply rails, have been used in order to isolate the two parts of the ASIC. The prototype chip holds 12 channels with 100um pitch and small variations in the building blocks from channel to channel, which share the same on chip biasing. The total area of the die is 3000x4000um².
The ASIC has been tested by injecting charge pulses at its input and simulating the capacitive effects of the detector with capacitors placed between the input of the preamplifier and ground. By placing decoupling capacitors on the testing board, the applied voltage steps in its input are becoming charge pulses. Fig. 8 depicts the measured transient response at the output of the amplifier for an input charge of 2fC. The overall gain of the chain is reduced due to the buffering scheme used on the testing board, which provides a gain of 0.9. Furthermore, a slight increase in the peaking time is also noticed due to the same reason. The analog output of the front-end electronics exhibits a peaking time of 45ns. The measured gain is 110mV/fC and remains almost constant for typical values of input charges, 1-8fC. Due to the AC coupling, the system is insensitive to DC level shift of the analog output.

The ENC has been measured by changing the value of the detector simulating capacitors. The r.m.s. value of the output voltage fluctuations was measured with an oscilloscope and the ENC was calculated by dividing this noise level by the overall gain of the chain. Fig. 9 shows the Equivalent Noise Charge (ENC) vs the detector capacitance. The calculated noise relationship is $350 + 55e_-/pF$ resulting in $460e_-$ rms for the 2pF detector capacitance.

6. SUMMARY

A new front-end stage has been designed for use in a luggage inspection system based on a linear array of CdTe sensors. The read-out chain, which is based on the voltage mode architecture, consists of a charge amplifier, a polarity select circuit, a semi-Gaussian shaper, a voltage amplifier and a discriminator. A multi-channel prototype, including also DACs for fine adjustment of the discriminator threshold, has been fabricated in a 0.6um CMOS process. The measured gain of the chain is 110mV/fC while the peaking time is 45ns. The measured ENC for the case of 2pF detector capacitance is 460e-. Finally, the power consumption per channel is 8mW.

7. REFERENCES