New configuration memory cells for FPGA in nano-scaled CMOS technology

Arash Azizi Mazreah a, Mohammad T. Manzuri Shalmani b,*

a Department of Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran
b Department of Computer Engineering, Sharif University of Technology, Tehran, Iran

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ABSTRACT

In nano-scaled CMOS technology, the reduction of soft error rate and leakage current are the most important challenges in designing Field Programmable Gate Arrays (FPGA). To overcome these challenges, based on the observations that most configuration bit-streams of FPGA are zeros across different designs and that configuration memory cells are not directly involved with signal propagation delays in FPGA, this paper presents three new low-leakage and hardened configuration memory cells for nano-scaled CMOS technology. These cells are completely hardened when zeros are stored in the cells and cannot flip from particle strikes at the sensitive cell nodes. These cells retain their data with leakage currents and positive feedback without a refresh cycle. Simulation results show that the proposed cells are working correctly during their configuration and idle cycles and that our cells have a lower soft error rate and leakage current in 22-nm as well as in 65-nm technologies.

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1. Introduction

Devices in CMOS technology have been scaled down aggressively with each technology generation to achieve a higher integration density and performance [1]. However, the leakage current has increased drastically with technology scaling and has become a major contributor to the total IC power [1]. Furthermore, as the feature sizes of devices and the supply voltage in CMOS technology were scaled down, the probability of soft errors increased. Soft errors are radiation-induced faults that occur because of a particle hit, either by an alpha particle from impurities in the packaging material or a neutron from cosmic rays [2].

Field-programmable gate arrays (FPGA) are ideal for implementing any type of digital system because they are reconfigurable and can be programmed to implement any digital logic [4]. Each FPGA involves an array of logic blocks that are connected through a network of routing switches that are all programmed by SRAM cells [4]. A six-transistor SRAM cell is conventionally used as the configuration memory cell [5]. As mentioned above, as the CMOS technology is scaled down, the total leakage current of chips increased. Furthermore, the total leakage current of a chip is proportional to the number of transistors on the chip, and because the configuration memory includes a large number of transistors on the FPGA chip, its leakage has also become a more significant component of total chip leakage in scaled CMOS technology. In addition, in scaled CMOS technology, the supply voltage and the nodal capacitance are reduced. Thus, an important drawback of SRAM-based FPGAs is that these devices are susceptible to single event upset (SEU) errors caused by cosmic particle strikes [6]. Therefore, the soft error rate and the leakage current of a configuration memory cell are the two most important parameters in designing configuration memory cells for FPGAs in nano-scaled CMOS technology.

In response to the challenges of a conventional six-transistor SRAM cell, our objective is to develop a hardened SRAM cell with dual threshold voltage transistors to reduce the leakage current of the cell without significant area overhead. The rest of this paper is organized as follows. Section 2 describes the basic structure of an FPGA. Then, we propose new configuration memory cells in Section 3. Next, in Section 4, a particle strike to the new configuration memory cells is investigated. The leakage current of new configuration memory cells is investigated in Section 5. Section 6 explains a look-up table and routing switch based on the new cells. Section 7 presents a comparison with other related works. Finally, we summarize the key results in Section 8.

2. Background

Fig. 1 shows the basic and simple structure (island-style) of an FPGA [7]. As shown in the figure, each FPGA consists of an array of configurable logic blocks (CLB) and a network of routing switches. Each configurable logic block includes a cluster of lookup tables (LUT),

* Corresponding author. Tel.: +98 2166166632; fax: +98 2166019246.
E-mail addresses: a.azizi@srbiau.ac.ir (A.A. Mazreah), Manzuri@sharif.edu (M.T.M. Shalmani).

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and each lookup table includes a set of SRAM cells and a multiplexer, as shown in Fig. 2(a) [5]. Also, Fig. 2(b) shows a typical buffered FPGA routing switch [8]. Based on configuration data stored in SRAM cells, each input is routed to the output of the switch. Conventional six-transistor SRAM cell (CV 6T SRAM cell) is used as the configuration memory cell [5]. Fig. 2(c) shows circuit schematics of CV 6T SRAM cell.

The effect of SEU on SRAM-based FPGA can be classified into either a transient error or a permanent error [6,9]. SEUs can directly make transient errors on memory elements and change the contents of register files and flip-flops. These errors are called transient because they may be overwritten or corrected using error-detection and correction techniques. Thus, transient errors impact the user-defined logic and flip-flops of the FPGA [9]. In addition, SEUs can make permanent errors on an FPGA if they alter the contents of the configuration bits [9]. In this case, the configuration bit remains erroneous until the new configuration is downloaded into the FPGA [6,9]. Furthermore, to accommodate the logic that implements reconfigurability, FPGA flexibility is achieved at the cost of silicon area occupation [10]. As technology has progressed, the area constraint has become less restrictive; however, the large number of integrated transistors is a source of higher energy consumption than ASICs [10].

It was observed in [11,12] that the configuration bit-stream of FPGA contains 87% zeros across different designs. The main reason for the higher number of zeros is the large unused number of the routing bits. Also in the case of an FPGA, it can be noticed that SRAM configuration memories are not directly involved with signal propagation delay [10]. In the next section and based on the observations that most configuration data are zeros and the propagation delay of configuring data into SRAM cell has not had any effect on FPGA performance, we designed low-leakage hardened cells that are resistant to flipping caused by a particle strike, either from 0 to 1 or from 1 to 0.

3. New cell

Fig. 3 shows an equivalent circuit to develop an eight-transistor configuration cell using a supply voltage of 0.95 V in a 22-nm technology node. Hereafter, we refer to this cell as 'basic new cell' or 'basic new configuration memory cell'. Also, Table 1 lists the sizes of transistors and threshold voltage level in both types of configuration cell. For fair comparison, the sizes of transistors in basic new cell are set to be the same as the improvement-leakage new cell, but in general, sizes of transistors in basic new cell can be different from sizes of transistors in improved-leakage new cell.
When ‘0’ is stored in the cell during the idle mode, M5, M6, M7 and M8 are ON, and there is a positive feedback between the ST node and the STB node; therefore, the ST node is pulled to GND by M8, and the STB node is pulled to VDD by M5. When ‘1’ is stored in cell, nodes ST and STB have high and low voltages, respectively, and transistors M5, M6, M7 and M8 are all OFF. Fig. 4 shows the leakage current of the cell during the idle mode for data retention when ‘1’ is stored in both types of the cell. For data retention without the refresh operation, in the left side of cell the leakage current of access transistors (M1 and M2) that charge nodes ST and N1 must be greater than the sum of leakage current that discharge nodes ST and N1. In the right side of cell the leakage current of access transistors (M4 and M3) that discharge nodes STB and N2 must be greater than the sum of leakage current that charge nodes STB and N2. Therefore, following conditions must be satisfied on the left and the right side of cell for storing ‘1’.

**Left side:** Node ST : \( I_{DS-M1}(at \ V_{SD} = 0.1V) > 2I_{Gate-M7}(at \ |V_{GS}|) \)

\( = 0.75V \mid V_{GD} = 0.75V \mid + I_{Gate-AB}(at \ |V_{GS}|) = 0.1V \mid V_{GD} = 0.75V \mid + I_{Gate-M6}(at \ |V_{GS}| = 0.75V \mid V_{GD} = 0.75V) \)

\( + I_{Gate-AB}(at \ |V_{GS}| = 0.75V \mid V_{GD} = 0.75V) + I_{DS-M5}(at \ V_{SD} = 0.85V) \)

(1)

**Node N1:** \( I_{DS-M2}(at \ V_{SD} = 0.1V) > I_{Gate-M6}(at \ |V_{GS}|) \)

\( = 0.75V \mid V_{GD} = 0.75V \mid + I_{Gate-AB}(at \ |V_{GS}| = 0.1V \mid V_{GD} = 0.75V) \)

(2)

**Right side:** Node STB : \( I_{DS-M4}(at \ V_{SD} = 0.1V) > 2I_{Gate-M6}(at \ |V_{GS}|) \)

\( = 0.75V \mid V_{GD} = 0.75V \mid + I_{Gate-M5}(at \ |V_{GS}| = 0.1V \mid V_{GD} = 0.75V) \)

\( + I_{Gate-M7}(at \ |V_{GS}| = 0.75V \mid V_{GD} = 0.75V) + I_{DS-M5}(at \ V_{SD} = 0.85V) \)

(3)

![Circuit schematics of proposed configuration memory cell (basic new cell).](image)

**Fig. 3.** Circuit schematics of proposed configuration memory cell (basic new cell).

**Table 1**

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Improved-leakage new cell</th>
<th>Basic new cell</th>
<th>Transistor</th>
<th>Improved-leakage new cell</th>
<th>Basic new cell</th>
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</table>

Node N2 : \( I_{DS-M3}(at \ V_{SD} = 0.1V) > I_{Gate-M7}(at \ |V_{GS}|) \)

\( = 0.75V \mid V_{GD} = 0.75V \mid + I_{Gate-AB}(at \ |V_{GS}| = 0.1V \mid V_{GD} = 0.75V) \)

(4)

To satisfy the above conditions, when ‘1’ is stored in the cell during the idle mode, similar to the technique introduced in [13,14], we used the leakage current of access transistors, especially the sub-threshold current of access transistors, including \( I_{DS-M1}, I_{DS-M2}, I_{DS-M3} \) and \( I_{DS-M4} \). Therefore, to satisfy the above conditions, during the idle mode as shown in Fig. 4, the Bit-Line and the Bit-Line-Bar were maintained at VDD and GND, respectively. Also, because data were stored on the ST and STB nodes and most leakage current components exist on these nodes, as indicated in Fig. 4, to reduce the leakage currents that discharge the ST node \( (I_{DS-M3}) \) and charge the STB node \( (I_{DS-M4}) \) when ‘1’ was stored in cell, we used a high threshold voltage for M8 and M5 to reduce the sub-threshold currents of these transistors (in both types of cells). The sub-threshold current increases exponentially by decreasing the threshold voltage. The leakage currents of access transistors including M1 and M4 are greater than the leakage currents of the driver transistors M5 and M8, because these access transistors have lower threshold voltages. With this threshold voltage assignment, the HSPICE simulation results show that the above conditions are satisfied, and ‘1’ has been successfully stored in the cell without any refresh cycle. The HSPICE parameters were obtained from the latest Predictive Technology Models (PTMs) for the 22-nm technology node [15].

![Leakage current in idle mode when ‘1’ is stored in the basic new configuration memory cell.](image)
For area comparison purpose, Fig. 5 shows the layout of the basic new cell and the layout of the CV 6T SRAM cell (Fig. 2(c)) under scalable CMOS design rules. The CV 6T SRAM cell has the typical layout topology and is as compact as possible. The CV 6T SRAM cell requires a 416–66 area, whereas the basic new cell requires a 464–78 area. It is worth mentioning that these values are calculated in the worst case because we do not take into account the potential area reduction obtained by sharing with neighboring cells. Therefore, the basic new cell area is 10% greater than the area of the CV 6T SRAM cell using the same design rules. However, this area overhead is less important because as technology progresses, the area constraint becomes less restrictive than the area of the CV 6T SRAM cell using the same design rules. Based on layouts shown in Fig. 5, all of the technology nodes, process variations, channel length and channel width are modified randomly. The parasitic capacitances and resistances of the bit-lines and word-lines were included in the circuit simulation. For testing the correctness of configuration operation, the following scenario was applied to both types of the new 8-transistor SRAM cell: (a) configuring ‘0’ into the cell and then configuring ‘1’ into the cell and (b) configuring ‘1’ into the cell and then configuring ‘0’ into the cell. Figs. 6 and 7 show the simulated waveforms from applying the above scenario. Table 1 lists the parameters of transistors, which were used in circuit simulations.

Fig. 5. Area comparison. (a) Layout of the new configuration memory cell. (b) Layout of the CV 6T SRAM cell.

To verify the correct operation of the two types of the new configuration cell during a configuration cycle, we simulated both types of the new configuration cell using HSPICE with 0.95 V for supply voltage. The HSPICE parameters were obtained from the latest Predictive Technology Models (PTMs) for the 22-nm technology node [15]. Based on layouts shown in Fig. 5, all of the parasitic capacitances and resistances of the bit-lines and word-lines were included in the circuit simulation. For testing the correctness of configuration operation, the following scenario was applied to both types of the new 8-transistor SRAM cell: (a) configuring ‘0’ into the cell and then configuring ‘1’ into the cell and (b) configuring ‘1’ into the cell and then configuring ‘0’ into the cell. Figs. 6 and 7 show the simulated waveforms from applying the above scenario. Table 1 lists the parameters of transistors, which were used in circuit simulations.
Fig. 6. Simulated waveform of basic new configuration memory cell. (a) Configuring zero and then one. (b) Configuring one and then zero.

Fig. 7. Simulated waveform of the improved-leakage new configuration memory cell. (a) Configuring zero and then one. (b) Configuring one and then zero.
cell can successfully store ‘1’ even while considering the process variation. Similar waveform obtained for improved-leakage new cell.

4. Particles strikes

When a particle strikes the drain or source of an OFF transistor, it produces a transient current between the drain/source and the substrate; therefore, two states can be considered:

1. When the particle strikes the drain/source of OFF PMOS transistor. In this state, as the particle penetrates the bulk of the transistor, it loses its energy, creating minority carriers (free electrons and holes). These minority carriers may be collected by the drain/source diffusions, and a positive glitch is therefore injected to the stroked node, as shown in Fig. 9(a).

2. When the particle strikes the drain/source of an OFF NMOS transistor. In this state, as the particle penetrates the bulk of the transistor, its energy loss creates minority carriers (free electrons and holes). These minority carriers may be collected by the drain/source diffusions, and a negative glitch is therefore injected into the stroked node, as shown in Fig. 9(b).

When the particle strikes the drain/source region of an OFF transistor, the injected charge can be modeled by the following current pulse [17,18]:

\[
I(t) = I_0 \left( e^{-t/\tau_s} - e^{-t/\tau_p} \right)
\]

where the parameter \( I_0 \) depends on the amount of injected charge, \( \tau_s \) is the collection time constant of the junction, and \( \tau_p \) is the time constant for initially establishing the ion track. The time constants for exponentials depend on several process-dependent factors, and in this work, the time constants given in [19] were used:

\[
\tau_s = 1.64 \times 10^{-10} \text{ s} \quad \text{and} \quad \tau_p = 5 \times 10^{-11} \text{ s}
\]

We used the above current pulse to model a particle strike to a transistor.

When a particle strikes one node of a SRAM cell, it injects a positive or negative glitch. This glitch may flip the value of the memory cell. One important parameter to characterize the sensitivity of a memory cell to particle strikes is the critical charge \( Q_{crit} \). A particle strike to a transistor can be modeled as the current pulse. For a given current pulse waveform \( I(t) \), \( Q_{crit} \) is defined as the minimum time integral on \( I(t)dt \) that results in the cell flip [2]:

\[
Q_{crit} = \int_0^{t_f} I(t)dt
\]

where \( I(t) \) is the injected current caused by the particle strike and \( t_f \) is the time duration from when the particle strikes a sensitive node of the memory cell to when the cell starts to continue the flipping process [20].

4.1. Particles strikes in new cell

In this section, we used the current pulse with Eq. (5) to model a particle strike to a sensitive node. For example, when zero is stored in the cell and a particle hits the node ST, we use a current pulse at node ST to mimic particle-induced glitch. Fig. 10 shows basic new configuration memory cell when zero is stored in cell and a particle hits the node ST during idle cycle. In general, when the particle strikes a new SRAM cell, four states can be considered:

1) Zero is stored in the cell and a particle hits the ST node or STB node. (A) When the particle strikes the ST node, because the M1 transistor is OFF, the particle strike to the OFF PMOS transistor produces a positive glitch on the drain of the OFF PMOS transistor. However, this transient glitch has no effects on the STB node because there is no pull down transistor to discharge the STB node; therefore, the voltage of the STB node stays steady and the injected charge through the particle strike is discharged very quickly by the M8 transistor. (B) When the particle strikes...
Fig. 11. Simulated waveform of particle strike to new configuration cell, when zero is stored in cell. Particle strikes to (a) Node ST and (b) Node STB.

Fig. 12. Simulated waveform of particle strike to new configuration cell, when zero is stored in cell. Particle strikes to (a) Node N1 and (b) Node N2.
Fig. 13. Simulated waveform of particle strike to new configuration memory cell, when one is stored in cell. Particle strikes to (a) Node ST and (b) Node STB.

Fig. 14. Simulated waveform of particle strike to new configuration memory cell, when one is stored in cell. Particle strikes to (a) Node N1 and (b) Node N2.
the STB node, because the M4 transistor is OFF, the particle strike to the OFF NMOS transistor produces a negative glitch on the drain of the OFF NMOS transistor. However, this transient glitch has no effect on the ST node because there is no pull up transistor to charge the ST node; therefore, the voltage of the ST node stays steady and the missed charge caused by the particle strike is restored very quickly by the M5 transistor. Fig. 11 shows a simulated waveform of a particle strike to the ST and STB nodes when zero is stored in the basic new cell and the improved-leakage new cell.

2) Zero is stored in the cell and the particle hits the N1 node or N2 node. (A) When the particle strikes the N1 node, because the M2 transistor is OFF, the particle strike to the OFF PMOS transistor produces a positive glitch on the drain of the OFF

![Diagram](image)

**Fig. 15.** (a) Reduced-charge-sharing (RCS) version of basic new cell to reduce the possibility of upsets due to charge sharing by separating same potential adjacent nodes. (b) Layout of reduced-charge-sharing new cell.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Size (W/L)</th>
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<tbody>
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<tr>
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</tr>
<tr>
<td>M10</td>
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**Table 2**

Transistor size (W/L) and threshold voltage level in reduced-charge-sharing new cell.

![Waveform](image)

**Fig. 16.** Simulated waveform for configuration cycle of RCS new cell. (a) Configuring zero and then one. (b) Configuring one and then zero.
PMOS transistor. This positive glitch turns off transistor M5, and the STB node will be at a high-impedance state, so there is no transition on the STB node; therefore, the voltage of nodes STB and ST stays steady, and the injected charge from the particle strike is discharged very fast by transistors M6 and M8. (B) When the particle strikes N2 node, because the M3 transistor is OFF, the particle strike to the OFF NMOS transistor produces a negative glitch on the drain of the OFF PMOS transistor. This negative glitch turns off M8, and the ST node will be at high-impedance state, such that there is no transition on node ST; therefore, the voltage of nodes STB and ST stays steady, and the missed charge through the particle strike is restored very quickly by transistors M5 and M7. Fig. 12 shows a simulated waveform of a particle strike to N1 and N2 nodes when zero is stored in the basic new cell and the improved-leakage new cell.

3) One is stored in the cell and a particle hits ST node or STB node. (A) When the particle strikes ST node, because the M8 and M6 transistors are OFF, the particle strike to the OFF NMOS transistor produces a negative glitch on the drain of the OFF NMOS transistor. However, this transient glitch has no effects on the node STB because the transistor M6 is OFF and any transition on node STB cannot propagate to node N1; therefore, the voltage of STB stays steady. However, the voltage of node ST is reduced because of the injected glitch caused by the particle strike. The reduced voltage of node ST can be restored by a new configuration cycle with one data or leakage current of transistor M1. (B) When the particle strikes STB node, because the M5 and M7 transistors are OFF, the particle strike to the OFF PMOS transistor produces a positive glitch on the drain of the OFF PMOS transistor. However, this transient glitch has no effect on node ST because transistor M7

Fig. 17. Simulated waveform of particle strike to RCS new cell, when zero is stored in cell. Particle strikes to (a) Node ST, (b) Node STB, (c) Node N1 and (d) Node N2.
is OFF and any transition on the STB node cannot propagate to the N2 node; therefore, the voltage of node ST stays steady. However, the voltage of node STB is increased because of the injected glitch caused by the particle strike. The increased voltage of node ST can be discharged by a new configuration cycle with one data or leakage current of transistor M4. Fig. 13 shows a simulated waveform of a particle strike to ST and STB nodes when one is stored in the basic new cell and the improved-leakage new cell.

4) One is stored in the cell and a particle hits N1 node or N2 node. (A) When the particle strikes N1 node, because the M6 transistor is OFF, the particle strikes the OFF NMOS transistor produces a negative glitch on the drain of the OFF NMOS transistor. This transient glitch turns on transistor M5 and pulls up the STB node, such that transistor M6 is turned on, and because the voltage of node N1 is reduced to a low voltage because of the particle strike, the voltage of node ST is pulled to a low voltage through transistor M6; this causes transistor M7 to turn on and node N2 be pulled up by transistors M5 and M7. Therefore, the cell is flipped because of the particle strike. (B) When the particle strikes N2 node, because the M7 transistor is OFF, the particle strike to the OFF PMOS transistor produces a positive glitch on the drain of the OFF PMOS transistor. This transient glitch turns on transistor M8 and pulls down node ST, such that transistor M7 is turned on, and because the voltage of node N2 is increased to a high voltage because of the particle strike, the voltage of node STB is pulled to a high voltage through transistor M7; this causes transistor M6 to turn ON, and node N1 is pulled down by transistors M6 and M8. Therefore, the cell is flipped because of the

Fig. 18. Simulated waveform of particle strike to RCS new cell, when one is stored in cell. Particle strikes to (a) Node ST, (b) Node STB, (c) Node N1 and (d) Node N2.
particle strike. Fig. 14 shows a simulated waveform of the particle strike to N1 and N2 nodes when zero is stored in the basic new cell and the improved-leakage new cell.

Consequently, both the types of new cell cannot be flipped from particle strikes while storing zero. Also, when one is stored, particle strikes to node ST or node STB cannot flip the cells; however, the cells require a recovery cycle, as described above; in this same scenario, a particle strike to node N1 or N2 flipped the state of the cells. In the above simulation, the HSPICE parameters were obtained from the latest Predictive Technology Models (PTMs) for the 22-nm technology node [15]. Based on layouts shown in Fig. 5, all the parasitic capacitances and resistances of the bit-lines and word-lines were included in the circuit simulation.

4.2. Charge sharing

When a particle that has high energy strikes the drain or source of a MOS transistor, it affects multiple nodes of memory cell simultaneously through charge sharing [20]. When multiple nodes are affected simultaneously, basic new cell and improved-leakage new cell may flit like all zero-hardened memory cells [12,18] and all hardened memory cells [22–24] which already presented in previous works. The probability of such a failure depends on the location, magnitude, and duration of the transient glitch [22]. Charge sharing is a strong function of layout and distance between struck node and adjacent node [21]. In new cells, worst case happens when two adjacent nodes (ST and N1 or STB and N2) which have same potential are affected. Therefore, in order to reduce the possibility of upsets due to charge sharing, we can modify the designing of basic new cell by separating same potential nodes. Fig. 15 shows reduced-charge-sharing new configuration memory cell (we refer to this cell as ‘RCS new cell’). In this version of basic new cell for reducing charge sharing, same potential nodes are separated from each other. Table 2 lists the sizes of transistors and threshold voltage level in reduced-charge-sharing new configuration memory cell.

To verify the correct operation of RCS new cell during a configuration cycle, we simulated this cell using HSPICE with 0.95 V for supply voltage. The HSPICE parameters were obtained from the latest Predictive Technology Models (PTMs) for the 22-nm technology node [15]. For testing the correctness of configuration
operation, the following scenario was applied to this ten-transistor cell: (a) configuring ‘0’ into the cell and then configuring ‘1’ into the cell and (b) configuring ‘1’ into the cell and then configuring ‘0’ into the cell. Fig. 16 shows the simulated waveforms from applying the above scenario. Also, Figs. 17 and 18 show particle strikes to sensitive nodes of reduced-charge-sharing version of new configuration cell. As shown in these figures, RCS new configuration memory cell is completely hardened and cannot flip from particle strikes at the sensitive cell nodes. RCS new configuration memory cell has lower soft error rate than basic new cell and improved-leakage new cell, but RCS new cell has greater area and leakage current than basic new cell and improved-leakage new cell. Section 7 compares RCS new cell with other cells.

5. Leakage current

As mentioned in the introduction, CMOS device sizes and supply voltages are aggressively scaled down with each technology generation. To maintain performance, however, this has
required a corresponding reduction in the transistor threshold voltage [25]. Because the MOSFET sub-threshold leakage current exponentially increases with a reduced threshold voltage, the leakage power dissipation has grown to be a significant fraction of the overall chip power dissipation in modern deep-sub-micrometer processes [25]. The total leakage current is proportional to the number of transistors; because a large fraction of modern FPGA devices includes a large memory content, such as configuration memory cells and embedded SRAM, the leakage current of memory cells causes significant standby power dissipation in modern FPGA devices.

Because leakage depends exponentially on the threshold voltage, a simple and common technique for reducing leakage power would be to replace transistors with high threshold voltages [10,25]. However, this technique significantly affects delays; so it should be only used for noncritical circuits [10]. In the case of an FPGA, SRAM configuration memory cells are not directly involved with signal propagation delay [10]. Therefore, the SRAM configuration memory cells in an FPGA can be implemented using slow high-threshold transistors to reduce leakage current. Consequently, in developing new cells, we used the dual threshold voltage. Fig. 3 shows the basic new cell; this cell uses a low threshold voltage in all access transistors. To reduce further leakage current, we designed an improved-leakage new cell. Table 1 lists the parameters of transistors in improved-leakage new cell. In this cell, we used a high threshold voltage in access transistors, including M2 and M3; so when zero is stored in cell, sub-threshold leakage currents of M2 and M3 are reduced. However in this cell, during the configuration cycle, Word-Line1 and Word-Line2 were maintained at GND and $V_{DD} + V_{TN_{M3}}$, respectively. Section 7 compares the average leakage of different SRAM cells.

6. LUT and routing switch architecture

Fig. 19(a) shows an LUT architecture with a 4-bit input (LUT address) based on the new configuration memory cells. Also, Fig. 19(b) shows the routing switch architecture with 16 input paths. As shown in Fig. 19(a), Bit-Line and Bit-Line-Bar are shared between all configuration memory cells in LUT. In this LUT, during the configuration cycle, Write-Enable is activated and data-in and its compliment are placed on Bit-Line and Bit-Line-Bar, respectively. During the idle cycle, Write-Enable is inactive, and Bit-line and Bit-line-bar are maintained at $V_{DD}$ and GND, respectively.

As mentioned in Section 3, we used the leakage current of the access transistor for storing ‘1’ in the new configuration memory cells, and Bit-line and Bit-line-bar are maintained at $V_{DD}$ and GND, respectively. Now consider a bit-stream shown in Fig. 20(a). Assume that this bit-stream must be configured into the LUT shown in Fig. 19(a). When the first bit (one) is written into the SRAM0 of LUT, the next bits (zeros) must be written into SRAMs 1, 2, ..., 15 of LUT. Because the data of these SRAM cells are zero and

![Fig. 22. (a) Circuit schematic of the refresh configuration memory cell introduced in [12]. (b) Possible layout for the refresh configuration memory cell introduced in [12].](image)

![Fig. 23. (a) Circuit schematic of zero-hardened memory cell proposed in [26]. (b) Possible layout for zero-hardened memory cell proposed in [26].](image)
all the Bit-lines and Bit-line-bars of SRAM0...SRAM15 are maintained at GND and VDD for long periods of time, this may cause one stored in SRAM0 to be destroyed. Fig. 20(b) shows simulated waveforms applying the above scenario. As shown in these waveforms, after a short period of time where Bit-line and Bit-line-bar are maintained at GND and VDD, one that is stored in SRAM0 may be destroyed when configuring zeros into the other cell (SRAM1...SRAM15). The above situation may occur in configuring the configuration memory of a routing switch.

To avoid the above situation a LUT and a routing switch have been designed based on new SRAM cells. After every two successive zero bits in the bit-stream, an idle mode cycle is inserted to give time to the LUT and the configuration memory of the routing switch to recover the ones as shown in Fig. 20(c). Inserting the idle cycle in the bit-stream for each two successive zeros caused increase in the configuration delay, but it is not important because the configuration delay has no significant effect on the performance of the FPGA [9].

7. Discussion about related work

Based on the observation that most configuration bits are zeros across different designs, three configuration memory cells have been introduced in [11,12,25,26]. An improved asymmetric configuration memory cell was introduced in [11,25]. In this asymmetric cell, the critical charge improved when zero was stored in the cell using a dual threshold voltage. Fig. 21 shows the circuit schematic of this asymmetric cell. The proposed asymmetric cell also lowers the leakage current when zero is stored in cell. In this cell, only the critical charge increased when zero was stored, and a particle with sufficient energy can change the state of cell. Instead, in the memory cells presented in this work, when zero is stored in the

Fig. 24. Simulated waveform from configuring one and then configuring zero in the zero-hardened cell proposed in [26].

Fig. 25. (a) Circuit schematic of the hardened-refresh configuration memory cell introduced in [27]. (b) Possible layout for hardened-refresh configuration memory cell introduced in [27].

Fig. 26. Simulated waveform for changing the state of the memory cell presented in [27] due to high leakage current from Bit-Line to A1.
cells, a particle strike to a sensitive node of the cells cannot change
the state of the cells, as shown in Section 4. Therefore, the new cells
presented in this work have lower soft error rate than the asym-
metric cell presented in [11,21].

An asymmetric SRAM cell designed based on the observation that
most configuration bits are zero was introduced in [12]. Fig. 22
shows a circuit schematic and possible layout of this memory cell.

The main idea to develop this memory cell is eliminating the
feedback loop using a pass transistor that is controlled by refreshing
signal (M7 in Fig. 22(a)). In this cell, after the data is written to the
cell, its feedback loop is disconnected by turning off the pass
transistor. Nodes of the cell keep their logic values because of the
charge stored in the node capacitance [12]. As the charge decays
with time, a refreshing signal is used to turn on the feedback pass

| Table 3 |
| Critical charge and Soft Error Rate (SER) of different memory cells in a 22-nm technology node with supply voltage 0.95 V. |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| SRAM cells     | Critical charge | Soft error rate | Using refresh signal |
|                | ST 1 to 0       | ST 0 to 1       | STB 1 to 0      | STB 0 to 1      | N1 1 to 0       | N2 0 to 1       | A 0 to 1        | B 1 to 0        |                |
| CV 6T SRAM cell|                |                |                |                |                |                |                |                |                |
| FF             | 153fC           | 260fC           | 153fC           | 260fC           | –               | –               | –               | –               | 2561 FIT       |
| TT             | 134fC           | 257fC           | 134fC           | 257fC           | –               | –               | –               | –               | 2892 FIT       |
| SS             | 117fC           | 252fC           | 117fC           | 252fC           | –               | –               | –               | –               | 3248 FIT       |
| Asymmetric SRAM cell in [25] |                |                |                |                |                |                |                |                |                |
| FF             | 52fC            | 425fC           | 246fC           | 99fC            | –               | –               | –               | –               | 1025 FIT       |
| TT             | 30fC            | 431fC           | 345fC           | 78fC            | –               | –               | –               | –               | 543 FIT        |
| SS             | 37fC            | 440fC           | 463fC           | 72fC            | –               | –               | –               | –               | 303 FIT        |
| Zero-hardened refresh cell in [12] (pass is OFF-best case) |                |                |                |                |                |                |                |                |                |
| FF             | –               | –               | –               | –               | 57fC            | –               | –               | 23fC            | 0              | 3770 FIT       | YES            |
| TT             | –               | –               | –               | –               | 555fC           | –               | –               | 20fC            | 0              | 3873 FIT       |
| SS             | –               | –               | –               | –               | 549fC           | –               | –               | 14fC            | 0              | 4071 FIT       |
| Basic new cell |                |                |                |                |                |                |                |                |                |
| FF             | –               | –               | –               | –               | 68fC            | 69fC            | –               | –               | 0              | 3211 FIT       | NO             |
| TT             | –               | –               | –               | –               | 75fC            | 75fC            | –               | –               | 0              | 2676 FIT       |
| SS             | –               | –               | –               | –               | 86fC            | 83fC            | –               | –               | 0              | 2432 FIT       |
| Improved-leakage new cell |                |                |                |                |                |                |                |                |                |
| FF             | –               | –               | –               | –               | 61fC            | 63fC            | –               | –               | 0              | 3021 FIT       | NO             |
| TT             | –               | –               | –               | –               | 70fC            | 70fC            | –               | –               | 0              | 2790 FIT       |
| SS             | –               | –               | –               | –               | 81fC            | 77fC            | –               | –               | 0              | 2548 FIT       |
| Reduced-charge-sharing new cell |                |                |                |                |                |                |                |                |                |
| FF             | –               | –               | –               | –               | –               | –               | –               | –               | 0              | 0              | NO             |
| TT             | –               | –               | –               | –               | –               | –               | –               | –               | 0              | 0              | NO             |
| SS             | –               | –               | –               | –               | –               | –               | –               | –               | 0              | 0              | NO             |
| Hardened refresh cell in [27] |                |                |                |                |                |                |                |                |                |
| FF             | –               | –               | –               | –               | –               | –               | –               | –               | 0              | 0              | YES            |
| TT             | –               | –               | –               | –               | –               | –               | –               | –               | 0              | 0              | YES            |
| SS             | –               | –               | –               | –               | –               | –               | –               | –               | 0              | 0              | YES            |
| Low leakage cell in [28] |                |                |                |                |                |                |                |                |                |
| FF             | 159fC           | 245fC           | 187fC           | 189fC           | –               | –               | –               | –               | 163fC          | 2983 FIT       | NO             |
| TT             | 150fC           | 226fC           | 160fC           | 500fC           | –               | –               | –               | –               | 155fC          | 3526 FIT       | 1813FIT        |
| SS             | 138fC           | 187fC           | 130fC           | 700fC           | –               | –               | –               | –               | 137fC          | 4526 FIT       | 1916FIT        |
transistor momentarily to recharge the node capacitance [12]. This cell completely hardened when zero was stored in the cell, and it cannot flip from a particle strike, similar to our proposed cells. However, this cell uses a refresh signal, and this signal must be applied and routed to all configuration memory cells of the FPGA [12]. Therefore, each refresh cycle includes charging and discharging the load capacitance of the refresh line, and because the refresh line is routed for all configuration memory cells, the load capacitance of the refresh line is large, and significant dynamic power is dissipated in the refresh cycle. Furthermore, the cells presented in this work have lower leakage current than refresh cell presented in [12].

An eight-transistor hardened configuration memory cell is introduced in [26]. Fig. 23 shows the circuit schematic of this memory cell. However, this cell does not operate correctly during the configuration cycle. To investigate this issue, we consider the following scenario:

- Configuring the cell with one and then configuring the cell with zero.

Fig. 24 shows the simulated waveform of the above scenario. As shown in this waveform, configuring zero after configuring one cannot be performed successfully. The main reason for this failure is that when the cell is configured with one, the A node and B node are pulled to $V_{DD}$ and GND, respectively, through M7 and M8; however, when the cell must be configured with zero, there is not any driver to pull the A node and B node to GND and $V_{DD}$, respectively. Consequently, the cell cannot be configured with zero.

Another eight-transistor hardened configuration memory cell is introduced in [27]. Fig. 25 shows a circuit schematic and possible layout of this memory cell. As shown in Fig. 25, in this cell, the feedback loop is eliminated by using pass transistors M5 and M6 similar to refresh memory cell introduced in [12]. Furthermore, the gates of transistors M1 and M2 are separated to harden nodes A1 and A2 [23]. The value of nodes A1 and A2 could degrade over time when pass transistors M5 and M6 are OFF [27]. For solving this problem, the gate control voltages $V_P$ and $V_N$ are applied to the

Fig. 28. Average leakage current of different memory cells in 22-nm technology node with supply voltage 0.95 V.

Fig. 29. Layouts of new memory cells which are designed in Cadence environment: (a) proposed eight-transistor memory cell (size $= 3.36 \mu m^2$) and (b) proposed reduced-charge-sharing memory cell (size $= 5.5 \mu m^2$).

Fig. 30. Simulated waveform for configuration operation of new cells in commercial 65-nm CMOS technology with supply voltage 1.2 V (in improved-leakage new cell during configuration cycle, we use $V_{DD}$ for Word-Line2).
transistors M5 and M6 to restore the values of nodes A1 and A2 [27]. One manner to control the gates of M5 and M6 is using periodic refresh signal to turn on the feedback pass transistors (M5 and M6) momentarily to recharge the nodes A1 and A2.

However, [23] describes two problems of this memory cell. The first problem is that nodes A1 and A2 could easily lose their state due to the leakage current from Bit-Line, since the feedback loop from node STB to A1 and A2 is cut off by the two pass transistors, M5 and M6 [23]. Then, the high leakage current from A2 to Bit-Line or from bit-line to A2 can possibly change the state of the memory cell [23]. Fig. 26 shows the simulated waveform of the above scenario in memory cell presented in [27]. The second problem of this memory cell is high cost of signal distribution network of $V_P$ and $V_N$ since $V_N$ and $V_P$ must be applied to every single memory cell [23]. Furthermore, similar to refresh cell introduced in [12], when this cell uses periodic signal for $V_N$ and $V_P$, each refresh cycle includes charging and discharging the load capacitance of the $V_N$ and $V_P$ lines. Because the $V_N$ and $V_P$

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**Fig. 31.** Simulated waveform in commercial 65-nm CMOS technology for particle strike to sensitive nodes of new cells, when zero is stored in cells. Particle strikes to (a) Node ST, (b) Node STB, (c) Node N1 and (d) Node N2.
lines are routed to all configuration memory cells, the load capacitance of the $V_N$ and $V_P$ lines are large and significant dynamic power is dissipated in the refresh cycle.

Based on the observation that common data is zero, a low leakage eight-transistor SRAM cell is introduced in [28]. Similar to an asymmetric cell presented in [25], in this memory cell the leakage current improved when zero was stored in the cell. Fig. 27 shows a circuit schematic and possible layout of this memory cell. In this cell, the leakage current reduced when zero was stored, but a particle with sufficient energy can change the state of cell.

Instead, in the memory cells presented in this work, when zero is stored in the cell, a particle strike to a sensitive node of the cell cannot change the state of the cell.

Based on the simulation results obtained in this work, Table 3 shows the critical charge and Soft Error Rate (SER) of the new cells and all abovementioned cells. The failure rate of a cell due to particle strikes is known as the soft error rate and decreases exponentially with an increasing critical charge of the cell nodes [12]. The units of SER are Failure in Time (FIT). One FIT is one failure in one billion hours [12]. The following equation is

Fig. 32. Simulated waveform in commercial 65-nm CMOS technology for particle strike to sensitive nodes of new configuration memory cells, when one is stored in cells. Particle strikes to (a) Node ST, (b) Node STB, (c) Node N1 and (d) Node N2.
generally used to calculate the FIT of a memory cell [12,29]:

\[ \text{SER} \propto N_{\text{flux}} A_{\text{node}} e^{-Q_{\text{crit}}/Q_s} \]  

(9)

where \( N_{\text{flux}} \) is the intensity of the neutron flux, \( A_{\text{node}} \) is the area of the node and \( Q_s \) is the charge collection efficiency obtained from [30]. Also, Fig. 28 compares average leakage current of new memory cells and all abovementioned memory cells in a 22-nm technology node with supply 0.95 V.

We extend our simulations to verify the operation, susceptibility to particle strike and leakage current of new configuration memory cells in commercial 65-nm CMOS technology with supply voltage 1.2 V. Fig. 29 shows layouts of new configuration memory cells which are designed in Cadence environment. For testing the correctness of configuration operation, the following scenario was applied to new memory cells: configuring ‘1’ into the cell and next configuring ‘0’ into the cell and then configuring ‘1’ into the cell. Fig. 30 shows the simulated waveforms from applying the above scenario. Also, Figs. 31 and 32 show particle strikes to sensitive nodes of new configuration cells. As shown in these figures in commercial 65-nm CMOS technology, basic new cell and improved-leakage new cell cannot be flipped from particle strikes while storing zero. While one is stored, particle strikes to node ST or node STB cannot flip the cell; however, the cells require a recovery cycle, but a particle strike to node N1 or N2 may flip the state of the cell. Also, reduced-charge-sharing new configuration memory cell is completely hardened and cannot flip from particle strikes at the sensitive cell nodes. Fig. 33 compares average leakage current of different memory cells in commercial 65-nm CMOS technology with supply voltage 1.2 V. Table 4 lists parameters of transistors which used in circuit simulations.

![Fig. 33. Average leakage current of different memory cells in commercial 65-nm CMOS technology with supply voltage 1.2 V.](image)

![Fig. 34. Normalized area of different memory cells respect to CV 6T SRAM cell.](image)

<table>
<thead>
<tr>
<th>Transistors</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
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<tr>
<td>Improved-leakage new cell</td>
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Finally, Fig. 34 compares area of different configuration memory cells. In this work, we do not consider the configuration delay because the configuration delay does not significantly affect the performance of the FPGA [12].

8. Conclusion

With the aim of achieving a low leakage and highly reliable configuration memory cell for an FPGA, we developed two eight-transistor configuration memory cells and a ten-transistor configuration memory cell. The key observations behind our design are that most configuration bits are zeros across different designs in FPGA applications, and SRAM configuration memory cells are not directly involved with the signal propagation delay in FPGAs. The new cells retain their data with leakage current when there is not any positive feedback. Two eight-transistor new cells are zero-hardened, but the new ten-transistor configuration memory cell is completely hardened. Consequently, these new cells have low soft error rate. In worst case and in comparison with the conventional six-transistor SRAM cell in a 22-nm technology node, the average leakage current of the basic version of new cell, improved-leakage version of new cell and reduced-charge-sharing version of new cell is lower by 21%, 43% and 18%, respectively.

References