NBTI-Aware Power Gating for Concurrent Leakage and Aging Optimization

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ABSTRACT

Power and reliability are known to be intrinsically conflicting metrics: traditional solutions to improve reliability such as redundancy, increase of voltage levels, and up-sizing of critical devices do contrast with traditional low-power solutions, which rely on small devices and scaled supply voltages. The emergence of Negative Bias Temperature Instability (NBTI) as the most relevant source of unreliability in sub-90nm technologies has even exacerbated this incompatibility of the two metrics: NBTI manifests itself as an increase of the propagation delay over time, which adds up to the delay penalty introduced by most low-power design solutions. In this work, we show how the most widely adopted leakage reduction solution, that is, power-gating, can overcome this conflict, and how it can be used to naturally reduce the effects of NBTI on delay. Based on this important property, we present a methodology for NBTI-aware power gating that allows synthesizing low-leakage circuits with maximum lifetime.

Categories and Subject Descriptors

B.7 [Hardware]: Integrated Circuits

General Terms

Design

Keywords

NBTI, leakage, aging, power-gating

1. INTRODUCTION

One of the negative side effects of technology scaling has been the increased non-idealities of the manufactured devices. The most widely known type of non-idealities concerns the non-determinism of devices due to process variations [1, 2]. These variations, mostly due to random fluctuations of dopant atoms and to the imprecisionness of the manufacturing process, can be viewed as a sort of ‘time-zero’ deviation from the nominal behavior of devices.

A second, and more insidious, type of non-ideality is relative to time-dependent changes in the operating characteristics of devices [3]. These irreversible modifications are generally classified as “reliability issues” and only recently have received consideration in the CAD community. Many sources of time-dependent variations do exist [3]. Among them, the generation of interface traps under negative bias temperature instability (NBTI) in pMOS transistors has become the most critical reliability issues in determining the lifetime of CMOS devices [4][5].

NBTI occurs when a pMOS is negatively biased (i.e., a logic ‘0’ is applied to the gate of the pMOS, resulting in \( V_{gs} = -V_{DD} \)), and manifests itself as an increase of the threshold voltage with time, resulting in the reduction of drive current and noise margin, causing in turn a degradation of the delay of a device. Experimental data report variation of \( V_{th} \) of about 10-15% per year, depending on the target technology. The delay degradation follows the same trend, yet with a smaller scale. The actual amount of degradation depends on several parameters of a device, such as its logic function, threshold voltage, size, load, and operating temperature [4][6][7]. An even more important parameter is the actual time spent in the critical state for NBTI (the stress states), that is, when a logic ‘0’ is applied to the device inputs. In fact, when a logic ‘1’ is applied (the recovery state), NBTI stress is actually removed, resulting in a partial recovery (i.e., a decrease) of the threshold voltage. Clearly, the values of the signals in a realistic circuit will typically evolve between logic ‘0’ and ‘1’ over time, thereby alternating stress and recovery conditions.

This value-dependent behavior of NBTI is reminiscent of low-power design techniques, although the specific conditions of this dependence are different. Power is in general affected by circuit activity (or idleness, in the case of static power), whereas NBTI-induced aging is affected by a specific values of the circuit signals. Therefore, in general, aging due to NBTI and power require different circuit states in order to be reduced. This “functional” difference adds up to to the already mentioned intrinsic conflict between power and reliability, and further contributes to their incompatibility.

In this work, we try to bridge this gap by establishing an important missing link between low-power solutions (and, specifically, power-gating) and NBTI-induced aging effects. This link relies on the observation that disconnecting a logic block from the ground voltage (i.e., the conventional way of implementing power gating) using a switch (i.e., a sleep transistor) provides a natural way of reducing the NBTI effects. This electrical property, on which we will elaborate in Section 2.2.1, implies that when a circuit is in a sleep state it is intrinsically immune to NBTI-induced aging.
However, although power gating is always advantageous from the aging perspective, its actual effectiveness depends on its implementation. As a matter of fact, the application of power gating to a logic block increases its nominal delay (i.e., at time zero), as a consequence of the non-zero resistance of the sleep transistor when the circuit is active. Therefore, even if power gating reduces the NBTI-induced delay degradation over time, having a larger delay at time zero may result in a virtual benefit. The amount of delay penalty invested for the implementation of power-gating must therefore be weighted against the corresponding energy saving and the actual desired lifetime of the circuit. This indicates a natural tradeoff between the achievable leakage savings and lifetime.

The second contribution of this work consists of a NBTI-aware power gating methodology that is able to analyze these complex interactions between aging and leakage power. The proposed solution incorporates (i) the characterization of the library cells and of the sleep transistor, (ii) a timing analysis engine, and (iii) the extraction of the tradeoff curves, which play designers on address ageing-aware power-gating design. More specifically, this methodology helps designers to figure out the best sleep transistor configuration (i.e., the minimum sleep transistor size) in order to achieve maximum lifetime and optimal leakage/performance trade-off.

We implemented our tradeoff analysis an automated tool that leverage standard EDA tools in an industry-strength design flow, using an industrial 45nm technology. Results on a set of standard benchmarks shows, for a sleep probability of 80%, lifetime extensions of more than 2X, using an area overhead of 18%, and while still keeping a leakage reduction of 91%, with respect to the non-power-gated circuit.

2. BACKGROUND

2.1 NBTI Effects

From the physical point of view, NBTI is due to the generation of traps at Si/SiO$_2$ interface in negatively biased pMOS transistors at elevated temperature, resulting in their increase over time; this, in turn, translates into a progressive increase of the threshold voltage, which affects saturation current and therefore delay of a pMOS device. A detailed treatment of NBTI effects and models is out of the scope of this paper; we refer the reader to classical tutorial papers on NBTI [4][5]. Here, we limit ourselves to listing a few basic functional characteristics of NBTI that are essential for the understanding of the context of this work:

1. For a given set of technological parameters of a device (e.g., $L_{eff}$, $T_{ox}$), NBTI effects are mainly dependent on temperature (delay degradation increases with increasing $T$), supply voltage (delay degradation increases with increasing $V_{dd}$), threshold voltage (delay degradation increases with decreasing $V_{th}$). Therefore, each library cell instance has its own specific NBTI-induced curve of $V_{th}$/delay degradation in a multi-parameter space ($V_{dd}$, $V_{th}$, temperature, size and elapsed time). Therefore, a customized characterization of cell libraries is required for the estimation of delay.

2. The alternation of stress and recovery periods complicates the modeling of NBTI, since each single device should in principle be explicitly simulated by collecting the temporal profile of stress/recovery cycles. Things are even more complicated for generic gates, in which each pMOS device is connected to a distinct input with its own time-dependent waveform.

It has been shown ([7]) that a generic waveform can be modeled as a periodic one with the same amount of stress time, and that aging is independent of the frequency of the applied waveform. Together, these properties imply that it is the total stress time that matters, (rather than the actual waveform), thus allowing to use signal probabilities in the simulation for the evaluation of the effective aging.

Previous works on on NBTI in the EDA domain are mostly focused on providing models of the delay degradation that are suitable for usage in gate-level designs ([6, 7]). The first application of these models has been in timing analysis; the work of Wang et al. [8], in particular, have first addressed the problem of how to incorporate these models into standard static timing analysis engines.

The literature on techniques for reducing NBTI-induced degradation is however quite limited, and only few solutions have been appeared recently. A first class of solutions [9, 6] implements NBTI-tolerant circuits adopting a conservative design style (e.g., gate over-sizing), while other approaches directly acts on the variables that affect NBTI aging, namely $V_{th}$ and $V_{dd}$ [6, 10]. The NBTI-aware synthesis solution proposed in [10] are somehow exceptions in the sense that they target the reduction of the stress probability during logic synthesis, that is, when cells are not yet instantiated. However, previous works ignore the intrinsic relationship between power-gating and NBTI compensation, thus missing the optimum trade-off between lifetime and power consumption.

2.2 Power-Gating Basics

Power gating is a coarse-grain generalization of the MTCMOS technique in which a header and/or footer transistor (usually called sleep transistor (ST)) is inserted on the pull-up and/or pull-down network of a CMOS gate, respectively; the transistor is turned off when the gate is in stand-by mode, thus sensibly reducing the leakage current that flows in the supply-ground path. In this work we refer to a footer-based implementation, which is quite popular in the literature ([11][12]).

The implementation of power gating implies several architectural and circuit level issues, such as: the definition of the granularity of the blocks to which gating is applied (the clustering), the physical design of the sleep transistor, and the distribution of the virtual ground voltage to the cells. For details about these issues we refer the reader to the literature ([11][12]). One issue deserves however some elaboration because it is central to the problem discussed in this paper: the sizing of the sleep transistor. The size of the sleep transistor affects the performance of the gates connected to it. A small transistor slows down the circuit in active mode due to its high resistance (resulting in a high virtual ground voltage), whereas a large transistor implies a large area overhead and a significant energy cost during ON/OFF transitions, but smaller degradation of the delay. Thus, the problem of the sizing is driven by several conflicting constraints.

In the rest of this section we show how the aging dimension can be incorporated into to the sleep transistor sizing problem, by exploiting the benefits of one side effect of power gating.
2.2.1 Effects of Sleep Mode on Circuit State

It is a well-know fact that power-gating does not preserve the values of the nodes of the logic block that is gated. This poses some problems when (i) storing values of memory elements such as flip-flops, and (ii) interfacing power-gated to non power-gated regions [13]. These problems have been solved by either resorting to special types of memory elements or by proper design of the sleep transistor cell, respectively. In this work we consider the combinational portion of a design, and therefore neither of the above issues affects our analysis. For our purposes, it is important to observe the behavior of the internal nodes of a (footer-based) power-gated circuit when they are disconnected from the ground by the sleep transistor. Nodes that have logic value ‘1’ will keep their value, whereas nodes with value ‘0’, conversely, will become floating nodes. Both the virtual ground line and the ‘0’ nodes gets charged to the logic ‘1’ by the leakage current of the pull-up network of the cells [14]. The speed of this charge process will depend on the design of the sleep transistor cell. Using a proper pull-up boosting mechanism as shown in [15], the charge process can be made extremely fast (in the order of tens of cycles) so that we can safely assume that all nodes in the region quickly reach a logic ‘1’. As an example of this behavior, Figure 1 shows the value of this charge process when they are disconnected from the ground by the sleep transistor. Nodes that have logic value ‘1’ will stay unchanged, whereas signal b, which is at ‘0’ when the sleep signal is activated, goes to ‘1’ quite abruptly, and becomes very close to V_{dd} (1.1V) after about 1–2 μs. Clearly, after such an interval, all the gates of a gated circuit will not be subject anymore to NBTI-induced aging.

![Figure 1: Charging of Nodes as a Result of Entering Sleep Mode.](image1)

3. AGING OF POWER-GATED CIRCUITS

As already mentioned, NBTI induces an increase over time of the threshold voltage of a pMOS device, that can be approximated as follows [6]:

\[
\Delta V_{th} = K (\beta \cdot t)^{1/4}
\]

where \( K \) is a constant that lumps all the technological parameters (e.g., oxide electric field, thermal voltage, etc.), \( \beta \) is the stress probability, that is, the fraction of time the gate voltage is at the logic ‘0’, and \( t \) denote time. The term \( \beta t \)

Figure 2: Delay Increase Over Time as a Function of Stress Probability.

can be seen as the stress time. The \( \frac{1}{4} \) exponent assumes that the NBTI phenomenon is due to diffusion of \( H \) species (as opposed to \( H_2 \) species [4], for which a different exponent should be used).

The delay of a logic gate, using the alpha-power law, is approximately given by:

\[
d = \frac{C_L \cdot V_{dd}}{(V_{gs} - V_{th})^2}
\]

where \( C_L \) is the load capacitance, \( V_{gs} \) the gate voltage, \( V_{th} \) the threshold voltage, and \( \alpha \) a technology-related exponents that can be approximated to 1 for sub-90nm technology. If the threshold voltage increases over time, as described by Equation 1, the new delay \( d' > d \) becomes:

\[
d'(t) = d \cdot (1 + \frac{K \cdot (\beta \cdot t)^{1/4}}{V_{GT} - K \cdot (\beta \cdot t)^{1/4}})
\]

where the time dependency of \( \Delta V_{th} \) has been made explicit, and where \( V_{GT} = V_{gs} - V_{th,0} \) (\( V_{th,0} \) is the (nominal) threshold voltage at time 0). For the sake of illustration, Figure 2 plots the delay increase over time using Equation 3 as a function of \( \beta \), assuming a value of \( K = 10^{-5} \) (corresponding to a delay increase of about 15% after 3 years), and \( V_{GT} = 0.7 \) (i.e., \( V_{gs} = 1V \) and \( V_{th,0} = 0.3V \)). We assumed a nominal delay at time 0 of 10 units.

Let us now analyze the behavior of the circuit under power gating. As already discussed, we assume that the entire circuit is power gated. This comes at the cost of some delay penalty \( \gamma \), due to the on resistance of the sleep transistor.

The delay formula becomes then:

\[
d'_s(t) = d_s \cdot (1 + \frac{K \cdot (\beta \cdot (1 - P_{sleep}) \cdot t)^{1/4}}{V_{GT} - K \cdot (\beta \cdot (1 - P_{sleep}) \cdot t)^{1/4}})
\]

\( d_s = d \cdot (1 + \gamma) \) is the delay of the power-gated circuit at time 0, and \( P_{sleep} \) is the probability of the sleep signal. We notice how, based on the analysis of Section 2.2.1, in the formula, the complement of the sleep probability \( (1 - P_{sleep}) \) multiplies \( \beta \); this is equivalent to say that the time spent in the sleep state reduce the stress. We are doing a small approximation here, since we are assuming that the time spent in the transition from/to the sleep state are negligible; however, as seen in Section 2.2.1, this assumption is perfectly reasonable: the transition takes a few clock cycles, an infinitesimal quantity compared to the time horizon of NBTI analysis (years).

Figure 3 plots in the same diagram the delay increase of the original circuit for \( \beta = 0.5 \) (dashed curve), and the delay of the power-gated circuit (Equation 4, solid curves) for different values of \( P_{sleep} \) (0.7, 0.8, 0.9), and for a value of \( \gamma = 3\% \).
We notice that, although the delay curves of the power-gated circuit start at a higher value (i.e., 10.00), thanks to the recovery effect of the time spent during the low-leakage sleep state, the curves grow more slowly than the delay curve of the non-power-gated circuit. For instance, the curve for $P_{\text{sleep}} = 0.9$ crosses the dashed curve around $t = 10^2$ seconds (about 3 months). Clearly, the lower the sleep probability, the later the curve will cross.

From this first-order analysis, it is evident that there are three parameters that affect the behavior of the delay over time: $P_{\text{sleep}}$, $\beta$, and $\gamma$. The first two are however related to the characteristics (functional and structural, respectively) of the circuit, and should be regarded as constants for a given circuit. The only design variable is therefore $\gamma$. The latter parameter directly maps to the sleep transistor size [11]–[12]: Higher values of $\gamma$ imply a smaller sleep transistors (thus with smaller area). Values of $\gamma$ closer to 0 imply increased sleep transistor sizes with large overheads.

Section 4 will illustrate how we can play with this constraint to maximize life-time of low-leakage digital circuits.

## 4. NBTI-AWARE POWER GATING FLOW

### 4.1 Characterization of NBTI Effects

Today’s design kits do not provide designers with timing libraries that support time-dependent variations. The first step of our methodology is therefore the construction of models that support this feature. To this purpose, we implemented a SPICE-based flow for the analysis of the aging of CMOS library cells.

Similarly to standard timing libraries, we filled look-up tables containing the NBTI-induced delay degradation of each cell. The characterization is made under several operating conditions: Static 0-probabilities of the inputs, stress voltage (i.e., $V_{gs}$), temperature, and aging time. The characterization was run by using a dedicated SPICE-based aging analysis flow consisting of a two-phase simulation: the pre-stress simulation phase, in which we estimate the aging effects of the p-type transistors contained in the standard cell, and the post-stress simulation phase, where the stress information are integrated into the pMOS device parameters and the delay degradation of the cell is measured and stored in a dedicated LUT.

More precisely, depending on the properties of the gates' signal and the environmental variables, the pre-stress simulation computes the aging of the pMOS sleep-transistors based on HSPICE built-in aging models and technology parameters provided by the library provider. The aging information sampled during pre-stress simulation are then translated into threshold voltage degradation (i.e., $\Delta V_{th}$). During post-stress simulation, the NBTI-induced $V_{th}$ degradation is modeled using a negative voltage-source on the gate-terminal of pMOS transistors. After running both pre- and post-stress simulation we have a complete description of the NBTI-induced cell aging.

### 4.2 Exploration Framework

Figure 4 shows the implemented NBTI-aware exploration framework for power-gated circuits. After obtaining a synthesized circuit, a post-synthesis simulation is needed to extract the statistical information of all the internal nodes. This also encompasses the analysis of the idleness periods of the circuits and the extraction of the sleep signal temporal distribution (i.e., $P_{\text{sleep}}$). Those information, which are the actual inputs of the implemented framework, are used to extract and annotate the effects of NBTI.

Depending on the operating conditions (e.g., supply-voltage, temperature and elapsed time), and the static 0-probability of internal nodes, the NBTI-induced delay degradation of each standard cell is extracted (using the NBTI-aware timing library described in Section 4.1), and annotated onto the circuit netlist. The annotated netlist is then loaded in a standard Static Timing Analysis (STA) engine that provides timing information of the aged circuit.

The collected aging curves are finally used to evaluate the leakage/aging tradeoff by determining the sleep transistor size corresponding to the required lifetime or leakage saving. With the proposed methodology, the resulting power-gated circuit will exhibit extended lifetime compared to non power-gated circuits, yet spending the least amount of leakage energy saving.

Section 3 has provided and analytical justification of the property we want to leverage in our solution: Since the application of power gating comes at a cost of some delay penalty, this penalty must be weighted against the potential benefit it offers in terms of lifetime extension. On one hand, power gating is always beneficial in terms of aging: that is, the aging curve always grows more slowly than the non power-gated case (Figure 3). On the other hand, if the power gating penalty is too large, the aging curve of the power-gated circuit may intersect the one of the non power-gated circuit at a time that is well beyond the typical lifetime of a circuit. This situation is shown in Figure 5, where the effects of $\gamma$ are
shown for an example $\beta = 0.5$, $P_{\text{sleep}} = 0.8$ case, in which we assume an observation window of $10^5s$ (about 3 years).

Figure 5: Delay Increase as a Function of Power Gating Delay Overhead.

It is clear from the plot that only values of $\gamma$ below 5% (dashed curves) do allow exploiting the natural recovery effect of the sleep state within the chosen observation window: curves for $\gamma = 7.5\%$ and $\gamma = 10\%$ do not cross the baseline delay curve of the non-power-gated design well beyond the observation window; actually, these solutions exhibit a larger delay than the non-power-gated design at $t = 3 \cdot 10^5s$.

It is worth re-emphasizing that, since a given value of $\gamma$ implies a sleep transistor width, it does not just results in a delay penalty, but also in (i) an area overhead (smaller transistor $\rightarrow$ larger transistor $\rightarrow$ larger area), and (ii) extra leakage power (smaller transistor $\rightarrow$ more extra leakage). These quantities must be taken into account in the exploration, and in particular leakage power, which is the reason why power gating is applied.

In a typical design flow, the exploration of the aging/leakage/area tradeoff is based on a scenario slightly different from the one depicted in Figure 5; the designer defines some guard-band delay increase with respect to the nominal delay, and lifetime is measured as the time at which the aging curve crosses the guard-band value.

For example, with reference to Figure 5, if this guard-band is 10%, lifetime of the non-power-gated circuit would be around $3 \cdot 10^5s$ (where the curve crosses the $1.10E+01$ grid-line – the dotted vertical line). In this case, only the solution with $\gamma = 2.5\%$ would manage to extend the lifetime, since it crosses the 10% delay guard-band at $t = 10^5s$. Nevertheless, we see from the plot that there exist other solutions with a value of $\gamma$ between 2.5% and 5% that can still extend the lifetime of the circuit (by a smaller value, yet with different costs of extra leakage and area).

What our exploration engine provides is precisely such a tradeoff analysis of the lifetime/area space. We use the relation between $d_P(t)$ and $\gamma$ expressed by Equation 4 as a tradeoff equation between aging and sleep transistor size, and thus leakage and area: a smaller $\gamma$ extends circuit lifetime thanks to intrinsic power-gating induced NBTI reduction, whereas a larger $\gamma$ reduces the leakage loss and the area overhead due to sleep transistor insertion.

5. EXPERIMENTAL RESULTS

The proposed NBTI-aware power-gating methodology has been implemented using standard EDA tools and an industrial 45nm design kit provided by STMicroelectronics as basis. Benchmarks, taken from the ISCAS85 suite, have been synthesized and mapped using Synopsys Design Compiler. The statistical information of the internal circuit nodes was obtained using Mentor Graphics’ ModelSim, using dedicated testbenches that emulate actual workloads; both switching activities and static signal probabilities have been annotated in Synopsys PrimeTime, which allowed detailed extraction of the statistics of the internal nodes for NBTI effects evaluation.

The characterization procedure described in Section 4.1 was done on a subset of the full cell library consisting of an inverter (INV), 2- to 4-input NAND, and 2- to 4-input NOR. All the supported driving strengths have been considered for each cell. As already described in Section 4.2, once we obtained the synthesized circuit netlist, the NBTI-induced delay degradation is calculated using a standard static timing analyzer, properly interfaced in order to read the modified, NBTI-aware libraries.

Concerning the power gating engine, in this work we consider an approach in which the entire circuit is connected to distributed sleep transistor cells (complete power gating). Since the sizing of the sleep transistor depends on the maximum current drawn by the block to be gated, we used the efficient method of [16] to obtain a tight upper bound for the maximum drawn current.

As an example result of the tradeoff analysis provided by our framework, Figure 6 shows the output of the exploration for benchmark c1908. We have used a delay guard-band value of 15% extra delay over the nominal delay (without power gating) to determine lifetime.

Figure 6: NBTI-Induced Delay Degradation for c1908 After 3 Years.

The plot shows lifetime values versus the leakage saving resulting from the application of power gating. Tradeoff curves are built by extrapolation of four points, corresponding to values of $\gamma$ of 2.5, 5, 7.5, and 10%; there is a curve for each value of $P_{\text{sleep}} = 0.4, \ldots, 0.9$. The vertical dashed line denotes the lifetime of the original, non-power-gated circuit (2.66 years for this benchmark). Leakage figures refer to the leakage power saved thanks to the application of power gating. The saving is ideally 100%, that is, we assume that when disconnected from the ground the gated logic consumes zero leakage. Clearly, the sleep transistor itself has some leakage that is proportional to its size; therefore, even a very large value of $\gamma$ will have a non-zero leakage penalty (or leakage saving smaller than 100%).

This plot can be used as follows: after extracting the actual $P_{\text{sleep}}$ from simulation, the designer will choose, on the
corresponding $P_{\text{sleep}}$ curve, the point corresponding either to the desired lifetime extension (resulting in a given leakage saving) or to the desired leakage saving (resulting in a given lifetime extension). For the case depicted in Figure 6, supposing that we want to extend the lifetime to 4 years, the curves say that we must have a value of $P_{\text{sleep}} > 0.8$. If $P_{\text{sleep}} = 0.8$, we must sacrifice a significant amount of leakage (89% saving – the bottom point of the $P_{\text{sleep}} = 80\%$ curve), using a small value of $\gamma$. If $P_{\text{sleep}} = 0.9$, the same lifetime target can be obtained by having a 95% leakage saving (a value slightly larger that $\gamma = 5\%$).

It is also worth mentioning that dynamic power does not represent an issue here. Previous works on power gating have also taken into account the fact that the switching of the sleep transistor dissipates dynamic power proportional to its size; in our case, however, we should look at the problem from an energy perspective. In order to make the application of power gating effective, we should guarantee that the idle bursts are long enough (e.g., in the order of thousands of cycles [11, 12, 15]); this means that we should expect that the switching probability of the sleep signal should be very small (< $10^{-3}$). Therefore, although there is some dynamic power cost in turning on the sleep transistor, this is a very occasional event, and the total energy is thus dominated by the leakage component.

Table 1 summarizes the results for all the ISCAS85 benchmarks in terms of lifetimes extension versus area overhead and leakage saving. For the sake of space, we only report figures for the extreme values of $\gamma$ (2.5% and 10%), corresponding to the extremes of the tradeoff curves of Figures 6. Values refer to a $P_{\text{sleep}}$ of 0.8.

### Table 1: Results on ISCAS85 benchmarks.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Lifetime - noPG (yrs)</th>
<th>$\Delta$Area [%]</th>
<th>$\Delta$Leakage [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>w/ PG</td>
<td>w/ PG</td>
<td>w/ PG</td>
</tr>
<tr>
<td>c041</td>
<td>2.95</td>
<td>6.79</td>
<td>0.31</td>
</tr>
<tr>
<td>c009</td>
<td>1.54</td>
<td>3.86</td>
<td>0.56</td>
</tr>
<tr>
<td>c080</td>
<td>1.60</td>
<td>2.21</td>
<td>0.47</td>
</tr>
<tr>
<td>c1355</td>
<td>5.86</td>
<td>9.23</td>
<td>0.81</td>
</tr>
<tr>
<td>c1908</td>
<td>2.66</td>
<td>4.25</td>
<td>0.52</td>
</tr>
<tr>
<td>c2075</td>
<td>1.80</td>
<td>3.42</td>
<td>0.61</td>
</tr>
<tr>
<td>c5340</td>
<td>1.96</td>
<td>3.77</td>
<td>0.52</td>
</tr>
<tr>
<td>c6315</td>
<td>0.97</td>
<td>2.15</td>
<td>0.44</td>
</tr>
<tr>
<td>c0285</td>
<td>1.42</td>
<td>2.31</td>
<td>0.50</td>
</tr>
<tr>
<td>c1752</td>
<td>2.10</td>
<td>2.97</td>
<td>0.42</td>
</tr>
<tr>
<td>avg.</td>
<td>2.19</td>
<td>4.57</td>
<td>0.54</td>
</tr>
</tbody>
</table>

Column Lifetime - noPG is the lifetime of the original, non power-gated circuit, defined as the time required by the circuit to degrade its performance of 15% beyond its nominal value. Column Lifetime - with PG show the range of lifetime values resulting from the application of power gating with different amount of “effort”. As already shown on the plots of Figure 6, too large a $\gamma$ will imply a too high initial overhead, resulting in exceeding the guard-band delay earlier than the non power gated circuit. Conversely, using a larger sleep transistor ($\gamma = 2.5\%$), we are able to extend the lifetime by more than 2X on average. This comes of course at the cost of extra area (18% on average – Columns $\Delta$Area) and reduced leakage savings (Columns $\Delta$Leakage). Leakage figures must be read as savings with respect to the leakage of the non-power gated design.

With the proposed exploration framework is therefore possible, depending on the required lifetime extension or leakage reduction, to determine the optimal value of the corresponding metric.

### 6. CONCLUSIONS

NBTI effects pose critical challenges for the reliability of circuits realized in sub-100nm technologies. In this work we explored the possibility of exploiting low-power techniques for concurrent leakage and aging optimization. We showed how power-gating provides a natural way of reducing NBTI effects, thus increasing the life-time of digital circuit. We also proposed a novel exploration framework which provides the designers with new tips for achieving the best trade-off between leakage and life-time extension. Experimental results conducted on a set of benchmarks mapped into an industrial 45nm technology shown as a dedicated NBTI-aware power gating may enlarge the duration of digital circuit, with minimal reduction in the leakage benefits with respect to a conventional power-gating scheme.

### 7. REFERENCES

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