EVALUATION BOARD FOR FREQUENCY HOPPING-CDMA SYSTEMS

Anael SAM, Vladimir STOFANIK, Igor BALAZ

Department of Radio and Electronics, FEI, STU, Ilkovicova 3, 812 19 Bratislava, Slovak Republic
E-mail: sam@kre.elf.stuba.sk, stofanik@kre.elf.stuba.sk, balash@elf.stuba.sk.

Abstract

An evaluation board with FPGA (XC2S15) and 200MHz single-chip Direct Digital synthesizer (AD9857) has been designed to demonstrate a Fast Frequency Hopping CDMA (FFH-CDMA) implementation. The paper shows how the pseudo-random Gold code may determine the frequency hopping of the carrier in FFH-CDMA systems.

Introduction

Universal Mobile Telecommunication System (UMTS) is currently under deployment. UMTS is experiencing growing interest for service providers, potential customers and subscribers. UMTS supports various multimedia services, which require wide frequency bandwidth to deliver the information content. Bearing in mind the fact that frequency resources are limited and expensive, systems enabling efficient utilization of the available frequency bandwidth and fast dynamic resource allocation are vital. In today's wireless communication systems it is inevitable to optimize frequency spectrum resources utilization. In UMTS, an efficient Wide-band Code Division Multiple Access (W-CDMA) is mostly utilized. CDMA technique, in general, permits many different signals to be co-located in the same frequency band and is capable of combating interference such as adjacent channel interference by using pseudo-random noise (PN) codes with minimum cross correlation. Frequency diversity is another advantage of systems utilizing CDMA technique. In a system, where CDMA has been applied, unauthorized signal demodulation and detection is difficult and hence the system achieves more privacy.

This paper introduces evaluation hardware with the possibility of fast switching (hopping) between the set of carrier frequencies. PN code with minimum cross correlation, e.g. Gold code, may be used to control the switching similar as in the FFH-CDMA systems. This is an alternative way of how the interference can be minimized.

Description of the evaluation board

The simplified block diagram of the evaluation board, we have designed, is shown in Fig. 1. It has been the aim of the authors to extend the resolution of the evaluation board used in [3], [4] and [5]. The new evaluation board has been designed to demonstrate spectral properties of frequency-hopped and QAM/QPSK modulated signals, e.g. signals used within FFH-CDMA. The evaluation board comprises of reference crystal oscillator (48MHz), FPGA
(XC2S15), single-chip 200MHz DDS with QAM/QPSK modulator (AD9857). The board has 24 general I/O signals that may be used as digital data input for QAM/QPSK applied to the synthesized carrier. The FPGA may be configured through the standard IEEE 1149.1 (JTAG) interface, or from a dedicated configuration memory that is not shown in Fig. 1.

![Simplified block diagram of the designed evaluation board](image)

**Fig.1 Simplified block diagram of the designed evaluation board**

**Implementation of carrier frequency switching according to the Gold code**

Usually to reduce co-channel and adjacent interference in a spread spectrum system, the PN sequences with minimum cross-correlation values are used. Different users in the system are assigned with none-overlapping parts of the PN sequence. Since the PN codes are not perfectly orthogonal, they contribute to the noise in the system. If we assume that the spreading codes are mutually orthogonal, then the cross correlation value is zero. This is an ideal case, which in reality can not be fulfilled in any communication system, hence the noise introduction into the system. The Gold codes are a set of small cross correlation PN codes created by modulo-2 addition of outputs of two Linear Feedback Shift Registers (LFSR). Gold codes are usually described by two polynomials that indicate the LFSR structures to be implemented at a system level.

Two primitive polynomials of 41 degree (2) and (3) have been selected to form the UMTS Long Uplink Scrambling Gold Code (4):

\[
y_1(x) = x^{41} + x^{20} + 1 \quad (2)
\]
\[
y_2(x) = x^{41} + x^{3} + 1 \quad (3)
\]
\[
y(x) = y_1(x) \oplus y_2(x) \quad (4)
\]

Figure 2 below shows the simplified block diagram of FFH-CDMA implementation incorporating the designed evaluation board. Both LFSR1 and LFSR2 together with the exclusive-or gate represent the Gold code generator. The details of the used Gold code are described in [2]. Seven least significant bits of the Gold code sequence are used to select one carrier from the set of 128 different carriers. These seven bits are converted to parallel form in the shift register. The output of the register defines the address in the look-up table. The table stores 128 frequency-tuning words, which correspond to 128 carrier frequencies. Each frequency-tuning word comprises of 32 bits. The corresponding frequency-tuning word is shifted to the AD9857 via serial peripheral interface (SPI). The carrier switching is synchronized by the frequency update (FUD) signal. FUD synchronizes and determines the start of the frequency synthesis process.
All timing and frequency control signals are derived within the FPGA from the reference crystal oscillator. The QAM/QPSK modulation of the carrier is implemented directly according parallel data.

The hardware within the FPGA is described using Verilog HDL. The synthesized logical structure has been optimized for the XC2S15 - FPGA using the XILINX Web-pack ISE 5.1 software.

![Fig.2 Simplified block diagram of the switching between the carriers according to the Gold code using the evaluation board](image)

**Conclusions**

The described evaluation board enables the demonstration of the fundamental properties of signals utilized for FFH-CDMA. The implementation of Gold code generator within the XC2S15 FPGA is very efficient. Fast switching (hopping) between the carriers according to the Gold code is utilized in FFH-CDMA system with the aim of improving spectral efficiency of the frequency bandwidth in use.

The evaluation board can be used to:

- Elaborate the spectral properties of the synthesized signals with fast switching between the selected carrier frequencies.
- Implementation of QAM/QPSK modulation.
- Research on PN codes with minimum cross-correlation value.

The evaluation board is also implements LFSRs using SRL16 (Shift register LUT) primitive for FPGA resources efficient designs. Hence design methodology used in this system contributes to the FFH-CDMA system optimization.
References


