A NEW ENHANCED DIFFERENTIAL CMOS COLPITTS OSCILLATOR

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This paper represents a new enhanced Colpitts oscillator, which is designed based on \( g_m \)-boosting of a conventional Colpitts oscillator. The proposed topology increases the negative resistant and enhances the start-up difficulty of the conventional Colpitts oscillator. This enables the Colpitts oscillator to operate in low-power consumption. Moreover, the differential and balanced structure helps limit even-order harmonics and degrades the common mode noise effects in output. The proposed circuit is designed using 0.18 \( \mu \)m technology and is simulated under 1.8 V supply voltage in advanced design system (ADS). Simulations show the output phase noise of \(-140\) dBc/Hz at 1 MHz offset frequency when the operating frequency is 1 GHz.

Keywords: Colpitts oscillator; \( g_m \)-boosting; oscillation frequency; phase noise.

1. Introduction

Oscillators are important building blocks of any communication transceiver–receiver system. They have different functionalities and applications such as local oscillators for up-down conversion of the information-bearing signals, and carrier signal generators for modulations. Oscillators can be implemented in different structures for instance ring oscillators, LC-tank oscillators, distributed resonator based oscillators and voltage controlled. Fully integrated oscillators are very essential parts in any radio frequency (RF) integrated transceivers for carrier generation. Digital systems and also transceivers in modern communication systems need high purity oscillators for low jitter clock generation.1–4

Today, due to wireless communication growth, modern systems have to be designed with the compatibility of supporting different communication standards
and operating in different frequency bands. This results in a more complex design criteria and necessities for the integrated oscillators. For example, nowadays mobile phones support multiple standards, with the compatibility of covering different frequency bands and multiple communication standards (e.g., GSM, PCS/DCS).

The most important design challenges of a fully integrated CMOS LC voltage-controlled oscillator (VCO) are the phase noise and its power consumption. Widening the tuning range of VCO results in reduction of the LC tank quality factor, therefore a higher trans-conductance of the active network is needed, which in turns causes higher power consumption. Several optimized structures for oscillators and VCOs are designed to fulfill the need for low power and low phase noise. Among these architectures, the differential cross coupled oscillators attracted much interest due to their ease of implementation and differential output which results in a good phase noise behavior. On the other hand, the single ended Colpitts oscillators despite their superior phase noise performance were rarely used as integrated circuits because of their single-ended output and poor startup condition that leads to higher power consumption. Alternatively, the cross coupled differential oscillators have a higher loop gain with lower power consumption with poorer phase noise behavior.5

In order to overcome the difficult startup condition of the Colpitts oscillators, a new \( g_m \)-boosted differential Colpitts oscillator is proposed in this paper that enhances the startup condition and therefore minimizes the power consumption. The proposed Colpitts structure meets both of the phase noise and power requirements in RF integrated circuits.

The design procedure of the proposed topology through \( g_m \)-boosting technique will be explained in Sec. 2, followed by phase noise behavior analysis of the proposed oscillator in Sec. 3. Proposed VCO type circuit will be introduced in Sec. 4 and simulation results are presented in Sec. 5. We will then summarize the paper in Sec. 6.

2. Design Procedure

A conventional gate-drain (GD) feedback Colpitts oscillator is shown in Fig. 1(a). The circuit oscillates if the negative resistant seen from the GD terminal compensates the inductor losses.6

To achieve the condition needed for oscillation, we should calculate the impedance seen from the GD terminal. This impedance can be easily calculated using the small signal model of Fig. 1(b). By using Kirchhoff’s current law (KCL) at the nodes \( V_{gs} \) and \( V_D \):

\[
V_D = \left( \frac{g_m}{C_1 C_2 s^2} + \frac{1}{C_2 s} \right) I_{in}, \tag{1}
\]

\[
V_{gs} = -\frac{I_{in}}{C_1 s}. \tag{2}
\]
Therefore

\[ V_{in} = V_D - V_{gs} = \left( \frac{g_m}{C_1 C_2 s^2} + \frac{1}{C_2 s} + \frac{1}{C_1 s} \right) I_{in}. \]  

(3)

The impedance seen from the GD will be calculated as:

\[ Z = \frac{V_{in}}{I_{in}} = \left( \frac{g_m}{C_1 C_2 s^2} + \frac{1}{C_2 s} + \frac{1}{C_1 s} \right). \]  

(4)

Considering \( s = j\omega \), the real value of \( Z \) is

\[ \text{Re}\{Z\} = -\frac{g_m}{C_1 C_2 \omega^2}. \]  

(5)

Therefore, the oscillation startup condition can be written as follow, where \( R_L \) is the series resistant of the inductor.

\[ R_L - \frac{g_m}{C_1 C_2 \omega^2} = 0. \]  

(6)

From (5), in order to have a larger negative resistant, we should increase the \( g_m \) via choosing a larger value of \( I_b \), leading to undesirable higher power consumption. Therefore, the negative resistant should be increased through different method. Figure 2(a) shows the proposed \( g_m \)-boosted Colpitts oscillator topology. As seen, a negative resistant of \(-1/g_{m0}\) is added in drain to increase the negative resistant. Now from the small signal model of Fig. 2(a) and writing KCL at \( V_{gs} \) and \( V_D \) nodes, the impedance seen from the GD terminal will be calculated as

\[ Z = \frac{V_{in}}{I_{in}} = \left( \frac{g_m}{C_1 C_2 s^2 - g_{m0} C_1 s} + \frac{1}{C_2 s - g_{m0} s} + \frac{1}{C_1 s} \right). \]  

(7)
Also, the real value of $Z$ is

$$\text{Re}\{Z\} = \frac{-g_m}{C_1 C_2 \omega^2} + \frac{g_{m0}}{C_1} \frac{g_{m0}^2 + C_2^2 \omega^2}{C_1^2}.$$  \hfill (8)

From (6) and (8), the negative resistant of the proposed topology is larger than that of the conventional Colpitts oscillator, if the following condition is satisfied

$$g_m g_{m0}^3 - C_1 g_{m0}^2 C_2 \omega^2 < C_1^3 C_2 \omega^2.$$  \hfill (9)

It should be mentioned that in both Figs. 1(a) and 2(a) the oscillation frequency is defined by

$$\omega = \frac{1}{\sqrt{LC}}, \quad C = \frac{C_1 C_2}{C_1 + C_2}.$$  \hfill (10)

Fig. 2. (a) Proposed $g_m$-boosted Colpitts topology, (b) small signal model.

Fig. 3. Simulated effective real value of $Z$ for the conventional GD Colpitts oscillator of Fig. 1(a) and the proposed topology of Fig. 2(a) with $C_1 = C_2 = 4 \text{ nf}$, $g_m = 7.13 \times 10^{-3}$ mho.
The simulated real values of the impedances seen from the GD terminal of the conventional GD Colpitts oscillator and the proposed topology are plotted with respect to frequency in Fig. 3. As seen in this figure, the proposed topology has a larger negative resistant with respect to the conventional configuration and therefore it improves the startup condition and decreases the power consumption.\textsuperscript{8}

Figure 4 shows the final structure of the proposed enhanced differential oscillator. As seen, in this structure, the current sources are replaced by the cross-coupled PMOS transistors M$_3$ and M$_4$, which provide the negative resistant at drains of M$_1$ and M$_2$ and enhance the startup condition.

Also, replacing the current sources with cross-coupled transistors leads to differential oscillation and reduces the phase noise that will be discussed in Sec. 3.

3. Phase Noise Discussion

As seen in Fig. 4, the designed oscillator exploits the differential structure which reduces the effects of common mode noises like substrate noise on the output of the oscillator.\textsuperscript{5} In this section, we will compare the phase noise behavior of the proposed oscillator with the conventional GD Colpitts oscillator (Fig. 1) and the conventional LC oscillator of Fig. 5. By using the cross-coupled configuration in drains of M$_1$ and M$_2$ transistors, the oscillation amplitude can be increased up to $V_{DD}$ decreasing the phase noise.\textsuperscript{2} By referring to a general oscillator, it is known that the presence of a noise source between one of the oscillator nodes and ground causes a phase noise $L$ at the offset frequency $\Delta \omega$, given by\textsuperscript{1}

$$L(\Delta \omega) = 10 \log \left[ \frac{\Gamma_{\text{rms}}^2}{q_{\text{max}}^2} \frac{\Delta f}{2 \Delta \omega^2} \right],$$

(11)
where, $q_{\text{max}}$ is the maximum amount of the electrical charge that will be loaded onto the capacitance of the node, across an oscillation period. $i_n^2$ is the power density of the noise current and $\Gamma$ is the ISF of the noise source.\(^2\)

3.1. Comparison with the conventional GD Colpitts oscillator

In order to have a fair comparison, we suppose that both enhanced Colpitts and the conventional GD Colpitts oscillators have the same circuit parameters ($C_1, C_2, L, M, \ldots$). In this situation, the phase noise produced by the LC tank and the switch transistor ($M_1$ or $M_2$) is the same for both of the topologies. But, the most important phase noise difference of the two topologies is resulted from the bias current source in conventional Colpitts oscillator and the PMOS cross-coupled transistors in the proposed circuit. Assuming that the current source transistor in conventional GD Colpitts oscillator and the PMOS cross-coupled transistors have the same size, the amount of channel noise is the same in both of the topologies and is calculated from the following equation:

$$i_{\text{disp}}^2 = \frac{4kT\gamma g_{mp}}{C_13} f \left( \frac{1}{2} \right)\;,$$

where, $k$ is the Boltzmann constant, $T$ is the temperature and $g_{mp}$ is the transconductance of the PMOS transistor. Now, assuming that the current source PMOS transistor in conventional Colpitts oscillator operates in saturation region all the times, the trans-conductance of it can be assumed to be constant all the time and its ISF can be expressed as\(^9\):

$$\Gamma_{\text{bias}} = \sin \omega_0 t \;.$$  

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![Fig. 5. The conventional LC oscillator.](image-url)
But the cross-coupled PMOS transistor in the proposed topology has not a constant trans-conductance and its trans-conductance is expressed by the following equation

$$g_{mp} = K_p(V_{DD} - A \cos \omega_0 t - |V_{tp}|) = AK_p(\cos \theta - \cos \omega_0 t).$$  \hspace{1cm} (14)

Valid for $-\theta < \omega_0 t < \theta$ where $A$ is the oscillation amplitude and

$$\theta = \cos^{-1}\left(\frac{V_{DD} - |V_{tp}|}{A}\right).$$  \hspace{1cm} (15)

Therefore, the effective ISF for the PMOS cross-coupled transistors is expressed as:

$$\Gamma_{\text{eff(cross)}} = \sin \omega_0 t \sqrt{\cos \theta - \cos \omega_0 t}.$$  \hspace{1cm} (16)

The square rms value of $\Gamma_{\text{eff(cross)}}$ is calculated as

$$\Gamma_{\text{eff(cross)},\text{rms}}^2 = \frac{1}{2\pi} \int_{-\theta}^{\theta} \sin^2 \omega_0 t[\cos \theta - \cos \omega_0 t] d\omega_0 t$$

$$= \frac{1}{2\pi} \left[ \frac{1}{3} \cos^2 \theta \sin \theta + \frac{2}{3} \sin \theta - \theta \cos \theta \right].$$  \hspace{1cm} (17)

The square rms value of $\Gamma_{\text{bias}}$ can be easily calculated and is equal to 0.5. A typical plot of the $\Gamma_{\text{bias}}$ and $\Gamma_{\text{eff(cross)}}$ is shown in Fig. 6. As can be easily understood from the Fig. 6, the rms value of $\Gamma_{\text{bias}}$ is much larger than the rms value of $\Gamma_{\text{eff(cross)}}$. Therefore, as mentioned, since the proposed enhanced and the GD conventional topologies have the same circuit parameters, from (11), (13), (16) and Fig. 5, the

![Fig. 6. A typical waveform and ISF of the bias current and PMOS cross-coupled transistors of the GD Colpitts oscillator and the proposed enhanced oscillator.](image-url)
phase noise of the proposed enhanced Colpitts oscillator is smaller than the conventional GD Colpitts oscillator, resulting in superior phase noise behavior.

3.2. Comparison with the conventional LC oscillator

For having a comparison with the conventional LC oscillator, consider a conventional cross-coupled LC oscillator of Fig. 6. As seen, both of the proposed Colpitts topology and conventional LC oscillator circuits incorporate PMOS cross-coupled pairs in their structure that show a same phase noise behavior if the two oscillators have the same oscillation frequency and amplitude. The major phase noise difference comes from the difference in lower section of the circuits and LC tanks. If we design the Colpitts oscillator with inductors of \( L/2 \) where \( L \) is the inductor used in conventional LC oscillator then, for having the same oscillation frequency we should have

\[
2C' = \frac{C_1 C_2}{C_1 + C_2}. \tag{18}
\]

For calculation of the ISF associated with the inductors, we should substitute the noise current sources of inductors with an impulse current injected to the circuit. In this condition all of the circuit components will be neglected except capacitors. Considering this, the voltage jump due to impulse current of area \( \Delta Q \) in conventional LC oscillator is

\[
\Delta V_O = \frac{\Delta Q}{C'}. \tag{19}
\]

In the proposed Colpitts oscillator the amount of output voltage jump due to impulse current is

\[
\Delta V_O = \frac{\Delta Q}{C_2}. \tag{20}
\]

since \( C_2 \) is directly connected to the output nodes. From (18) we know that \( C_2 > 2C' \) therefore, from (19) and (20), the ISF associated with the inductors in proposed oscillator is smaller than the ISF of the inductor noise in conventional LC oscillator.

On the other hand, the proposed oscillator is composed of two Colpitts oscillators in lower section of the circuit whereas the conventional LC oscillator uses a NMOS cross-coupled pair. For comparing the phase noise associated with these parts, the ISF and transistor currents of Colpitts pair and NMOS cross-coupled pairs of the two oscillators are plotted in Fig. 7. As seen in this figure, in conventional LC oscillator, the pick points of transistor current and ISF almost overlap with each other resulting in a large \( \Gamma_{\text{eff}} \) whereas in the proposed Colpitts configuration, this overlap does not occur and the resulted \( \Gamma_{\text{eff}} \) has a smaller value which will lead to a smaller phase noise. From the physical point of view, this happens because there is a LC circuit between the outputs and gates of the NMOS Colpitts pairs that cause a phase difference between these voltages which in turn prevents the overlapping between the
The above analysis shows that the proposed Colpitts configuration has a better phase noise performance with respect to the conventional LC oscillator.

4. VCO Prototype of the Proposed Oscillator

In many applications such as phase locked loops (PLLs) we need a VCO. The proposed Colpitts architecture can be easily designed to act as a voltage controlled oscillator. This can be achieved by adding two varactors between the outputs (drains of the switch transistors $M_1$ and $M_2$). The designed VCO version of the proposed oscillator is shown in Fig. 8.
Because in differential oscillation $C_2$ is replaced by $C_{\text{var}}$, the oscillation frequency of the designed VCO is defined as:

$$\omega_{\text{osc}} = \frac{1}{\sqrt{LC}}, \quad C = \frac{C_1 C_{\text{var}}}{(C_1 + C_{\text{var}})}.$$  \hspace{1cm} (21)

5. Simulation Results

The proposed $g_{m}$-boosted enhanced differential Colpitts oscillator, the conventional GD Colpitts oscillator and the conventional LC oscillator were designed and simulated in ADS software. The parameters of the designed circuits are shown in Table 1. For a precise comparison the, three oscillators were designed using the same transistor sizes. It is worth mentioning that the $L$ and $C$ values of the conventional LC oscillator have been chosen based on the analyses of Sec. 3.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>CMOS 0.18 $\mu$m</td>
</tr>
<tr>
<td>$L$ (Colpitts configurations)</td>
<td>8 nH</td>
</tr>
<tr>
<td>$L$ (conventional LC configuration)</td>
<td>16 nH</td>
</tr>
<tr>
<td>$C$ (conventional LC configuration)</td>
<td>1.575 pF</td>
</tr>
<tr>
<td>$C_1$</td>
<td>6.3 pF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>6.3 pF</td>
</tr>
<tr>
<td>Switch Transistors (M1, M2) Size</td>
<td>15 $\mu$m/0.18 $\mu$m</td>
</tr>
<tr>
<td>Cross-coupled PMOS Transistors Size</td>
<td>30 $\mu$m/0.18 $\mu$m</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>1.8 V</td>
</tr>
</tbody>
</table>

Table 1. The design parameters of the proposed oscillator and the conventional GD topology.

![Fig. 9. Startup operation of the proposed differential Colpitts oscillator.](image-url)
Figure 9 shows a sample transient differential output waveform of the proposed oscillator. As it can be seen, the oscillator has a relax startup which is a superior performance with respect to the single output GD Colpitts oscillator.

Phase noise is the most important metric of an oscillator. The phase noise performances of the proposed Colpitts structure has been compared with the conventional GD Colpitts oscillator and the conventional LC oscillator theoretically in Sec. 3 and it has been shown that the proposed topology has a better phase noise performance due to a lower rms value of the ISF. Figure 10 shows the simulated

![Figure 10](image)

Fig. 10. Comparison between the phase noise of the proposed oscillator and the conventional GD Colpitts oscillator.

![Figure 11](image)

Fig. 11. Simulated tuning curve of the designed voltage controlled oscillator.
phase noises of the three oscillators. This figure proves our analysis of the phase noise behavior and the proposed topology shows a better phase noise behavior with respect to the GD Colpitts and conventional LC oscillators.

One important metric of a VCO is its tuning curve, plotted in Fig. 11 for the proposed topology. The tuning curve shows the output frequency range that the VCO can generate versus the input tuning signal. The slope of the tuning curve describes the tuning sensitivity $K_{VCO}$ which is an important parameter in designing of the RF building blocks such as PLLs. In the ideal cases, $K_{VCO}$ is a constant parameter but in practice it is not the case especially when the frequency is closed to the minimum or maximum of the tuning curve, as shown in Fig. 11.

6. Conclusion

In this paper, a new configuration for the MOS differential Colpitts oscillator is presented that has a better startup behavior than the conventional Colpitts oscillator. This is achieved through using a negative resistant in drain of the conventional GD Colpitts oscillator in place of the bias current. The VCO type of the proposed topology is also designed. The proposed oscillator circuit is analyzed from different aspects such as phase noise and startup condition. The simulations all show the better performance of the proposed new topology with respect to the conventional configuration.

References