JPE 11-5-2

A Current-Fed Parallel Resonant Push-Pull Inverter with a New Cascaded Coil Flux Control for Induction Heating Applications

Alireza Namadmalan†, Javad Shokrollahi Moghani*, and Jafar Milimonfared*

†* Dept. of Electrical and Electronics Eng., Amirkabir University of Technology, Tehran, Iran

Abstract

This paper presents a cascaded coil flux control based on a Current Source Parallel Resonant Push-Pull Inverter (CSPRPI) for Induction Heating (IH) applications. The most important problems associated with current source parallel resonant inverters are start-up problems and the variable response of IH systems under load variations. This paper proposes a simple cascaded control method to increase an IH system's robustness to load variations. The proposed IH has been analyzed in both the steady state and the transient state. Based on this method, the resonant frequency is tracked using Phase Locked Loop (PLL) circuits using a Multiplier Phase Detector (MPD) to achieve ZVS under the transient condition. A laboratory prototype was built with an operating frequency of 57-59 kHz and a rated power of 300 W. Simulation and experimental results verify the validity of the proposed power control method and the PLL dynamics.

Key Words: IH systems, Current Source Parallel Resonant Push-pull Inverter, cascaded control method, PLL Circuits

I. INTRODUCTION

Due to its high efficiency, precise control and low pollution properties, induction heating is widely used in industrial fields and in home appliances [1].

A large number of topologies have been developed in this area, among them the current-fed and voltage-fed inverters are the most commonly used [2]–[9]. An important advantage of voltage source inverters is the wide variety of control methods that they use to control output power, such as Pulse Frequency Modulation (PFM), Pulse Amplitude Modulation (PAM), and Pulse Density Modulation (PDM) [8]. A Current Source Inverter (CSI) has a limited number of control methods, but it is less affected by input voltage ripples and it has short circuited protection capability [2]–[5].

ZVS is critical for the reliable operation of standard current-fed parallel resonant inverters. Under steady-state conditions, ZVS can be achieved by using common techniques such as a PLL or other integral controllers [3]. There are two types of PLL circuits and the difference between them is based on the Phase and Frequency Detector methods (PFD). One of them is the Charge-Pump PFD (CP-PFD) and the other is the Multiplier Phase Detector (MPD). The latter has a fast dynamic response while having a nonzero phase error and the former has a poor dynamic response while having a zero steady state phase error [10]. Under transient intervals, ZVS will not be achieved using the CP-PFD method. As a result, in conventional current-fed parallel resonant inverters, the blocking diodes are required to prevent the internal body diode of the switches from conducting [3], [11]. However, these diodes will increase the conduction losses. Furthermore, a start-up problem may result in an overvoltage across the switches. In addition, during the start-up period the ZVS will not be achieved due to the poor dynamic of the CP-PFD circuit; and consequently a switch failure may occur. Therefore, to achieve ZVS under the start-up condition the input voltage must have a low slew rate to help the PLL circuit track the resonant frequency [3].

In this paper to eliminate the current and voltage overshoots at start-up, a new cascaded control method is proposed. In this method, the step response of the system is improved for a wide range of load variations while using a simple control method in comparison to robust and adaptive controllers [12], [13]. The net efficiency, the melting rate, and the output power of an IH system depends on the output current [2], so using a precise control method improves the practical indexes of an IH system.

In this study, a PLL circuit based on a MPD and its application to IH systems is analyzed. The PLL circuit can track the resonant frequency due to its fast dynamic response at start-up, so dynamic ZVS is achieved. This technique is proposed for IH applications where the work-piece is not ferromagnetic which results in a lower bandwidth for the

Manuscript received Sep. 19, 2010; revised Jul. 14, 2011
Recommended for publication by Associate Editor Tae-Woong Kim.
† Corresponding Author: namadmalan66@aut.ac.ir
Tel: +98-21-85-64543350, Amirkabir University of Technology
* Dept. of Electrical and Electronics Eng., Amirkabir University of Technology, Iran

resonant frequency deviation [2]. Comparing the experimental results of a MPD and a CP-PFD, the MPD method is shown to be the best choice since it can track the resonant frequency at start-up while the steady state phase error is negligible.

II. Principle of Operation

Fig. 1 shows two conventional current mode parallel resonant inverters using only two switches which are in series with two blocking diodes (D_1 & D_2). Unlike these conventional topologies, by achieving dynamic ZVS, the two switches from [3] do not need these blocking diodes. In this work, although both of the topologies, (a) and (b), can be implemented, it is preferred to use (b) for dc-dc converters [14], and (a) for induction heating applications or dc-ac converters because of their symmetrical current injection [15]. The proposed topology is a parallel resonant push-pull inverter or the (a) topology as seen in Fig. 1. The advantages of the push-pull method are its simple trigger circuits and the reduction in the number of switches for low and medium power applications in comparison with the full bridge topology [9], [11], and [15]. The inductances of L_1 and L_2 are much larger than the resonant inductor L_r, so under normal steady-state operation the dc-link current is approximately constant, and the switching network injects an alternating square-wave current into the resonant tank [9], [11]. In this circuit the two switches are operating with duty cycle that is slightly more than half (D>0.5) to achieve soft switching and to prevent the internal body diode of the power MOSFETs from conducting [9]. The inverter circuit turn-off angle or β [4] is fairly close to zero because the inverter is working in zero voltage and zero current switching (ZVZCS). Also, β is the phase difference between the resonant tank voltage and the injected current to the resonant tank.

For a push-pull circuit, the current of L_2 which is in series with S_2 is injected into the parallel resonant tank, and then returned to the dc-link when S_1 is on, when $0<t<T/2$. This process repeats for S_2 during the second half period, $T/2<t<T$, while the peak current of each switch is I_d, where I_d is the dc-link current of the CSPRPI shown in Fig. 1.

At the resonant frequency, the drain to the source voltage of each switch is like a half sine wave and the current of each switch is like a square wave. Fig. 2 shows the current and voltage waveform patterns of S_1 and S_2 when the inverter works in the ZVZCS condition. Fig. 3 shows the proposed CSPRPI without blocking diodes and a buck converter at dc-link side for output power conditioning. The phase locked loop (PLL) circuit tracks the frequency of soft switching under load parameter variations. The transfer function of the parallel resonant tank's impedance is derived by equation (1). By assigning a zero value to the phase of *z(s),* the frequency at which ZVZCS occurs can be derived by equation (2) as follows:

$$Z(S)=\frac{L_r s+R}{L_r C_r s^2+RC_r s+1}$$
$$\angle Z(j\omega_{in})=0 \;\Rightarrow\; \tan^{-1}\left(\frac{\omega_{in}}{2\xi\omega_n}\right)-\tan^{-1}\left(\frac{2\xi\omega_n\omega_{in}}{\omega_n^2-\omega_{in}^2}\right)=0 \tag{1}$$

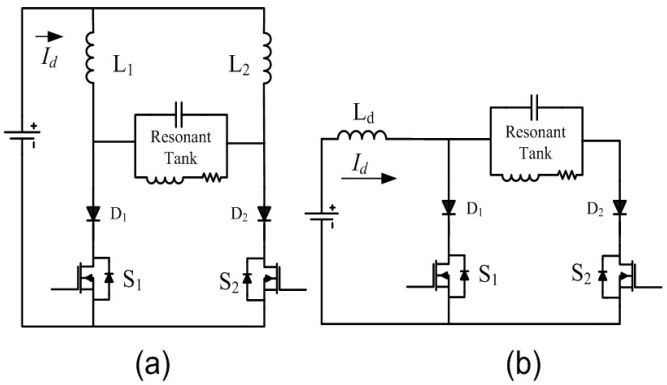

Fig. 1. The two conventional parallel resonant inverters.

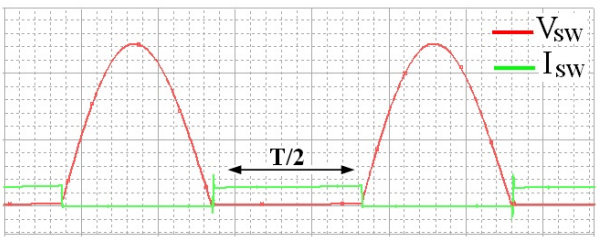

Fig. 2. The current and voltage waveforms of S_1 and S_2.

$$\xi=\sqrt{\frac{R^2C_r}{4L_r}},\ \omega_n=\frac{1}{\sqrt{L_rC_r}} \tag{2}$$
$$\Rightarrow \omega_r=\omega_n\sqrt{1-4\zeta^2}.$$

R, L_r, C_r, ω_n, and ω_r are the load resistance, the resonant inductance, the resonant capacitance, the natural frequency of resonant tank and the resonant frequency respectively. R is the sum of the coil resistance and the work-piece resistance referred to the primary or coil. ζ is the damping ratio of the parallel resonant tank circuit. Another important parameter that can be defined for a parallel resonant tank is the quality factor or Q as follows:

$$Q=\frac{\omega_r L_r}{R}. \tag{3}$$

According to [11], the inverter and the resonant tank can be modeled as an RLC load using the average model technique which is shown in Fig. 4, while the parameters of the proposed modeling are derived by equation (4). R_e is the load resistance referred to dc-link side. By comparing the push-pull topology with the full bridge scheme, R_{eq} in the full bridge scheme is four times the one in the push-pull topology for the same resonant tank [9].

$$L_{eq}=\frac{L_{1,2}}{2},\ R_{eq}=\frac{2}{\pi^2}(1+Q^2),\ C_{eq}=\pi^2C_r. \tag{4}$$

By assigning zero to the voltage integral of the dc-link inductors over one switching period, the output voltage to the dc-link voltage ratio K_V can be derived by equation (5) where V_d is the dc-link voltage.

$$\int_0^{2\pi}V_L d\theta=\int_0^{\pi}V_d d\theta+\int_{\pi}^{2\pi}(V_d-\hat{V}_o\sin\theta)d\theta=0$$
$$\hat{V}_o=\pi V_d \;\Rightarrow K_V=\pi. \tag{5}$$

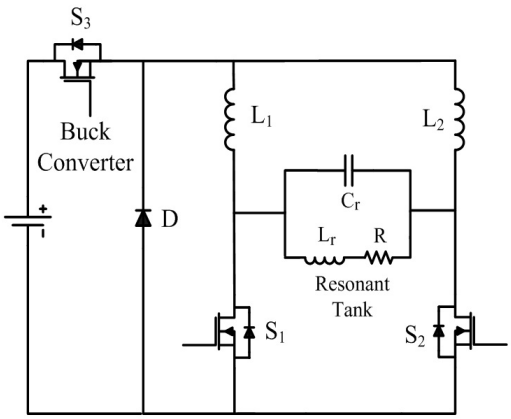

Fig. 3. The proposed CSPRPI with buck converter.

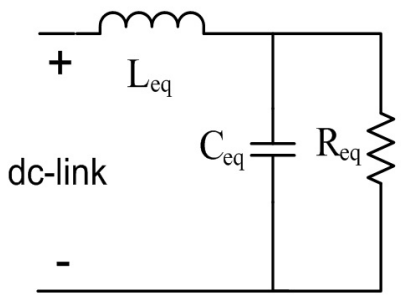

Fig. 4. The model of CSPRPI using average model technique.

In order to calculate the current ripple of the dc-link, the current is considered for a half period of the switching frequency. The second half of the switching frequency is repetitive which means that the ripple of the dc-link current will be twice the switching frequency. Accordingly, equation (6) formulates the dc-link current as a function of time for $0<t<T$.

$$i_d(t) = \int_0^t \frac{V_d}{L} dt' + \int_0^t \frac{(V_d - V_0)}{L} dt' + I_0. \tag{6}$$

Therefore, the current ripple (peak to peak) at the dc-link side is derived as follows:

$$\Delta i_d(t) = \int_0^t \frac{V_d}{L} dt' + \int_0^t \frac{V_d(1 - K_V Sin(\omega_r t'))}{L} dt'$$

$$\frac{\partial \Delta i_d(t)}{\partial t} = 0 \Rightarrow t_{\max} = \frac{\sin^{-1}(\frac{2}{K_V})}{\omega_r}$$

The ripple value is finally derived by equation (7). This equation shows the relationship between the inductances of the dc-link inductor, the operating frequency, and the ripple of the dc-link current.

$$\Delta I_{dc} \cong \frac{1.152 V_d}{2 L_{1.2} \omega_r}. \tag{7}$$

III. PLL Modeling

A PLL is a device which causes one signal to track another. It keeps the output signal synchronized with a reference input signal in the frequency as well as the phase. A PLL circuit consists of a Voltage Controlled Oscillator (VCO), a Phase Detector (PD), and a Loop Filter (LF) [16].

In this paper a simplified PLL circuit is implemented which has a simple structure and is less expensive. The PLL circuit has one Potential Transformer (PT) that senses the output voltage. As mentioned in the principle of operation section, the triggering signal will be in phase with the current injected into the resonant tank. Therefore, by comprising the output voltage and the instant triggering signal, the phase error signal between the resonant tank voltage and the injected current is produced. To accomplish the comprising process, the output voltage must be rectified in a half wave shape and then passed through a chopper circuit to shape the output voltage to a square-wave with a 50% duty cycle. The proposed PLL circuit with the PT and triggering circuits are shown in Fig. 5. According to Fig. 5, the pulse shaping circuit makes a proper overlap at about 200 ns for an operating frequency of 58 kHz.

In this paper to implement the PLL circuit, an HC/HCT4046A Integrated Circuit (IC) is used which consists of a VCO and three Phase Detector (PD) modes [17]. Here, the phase detector is based on mode-2, which has a tri-state logic characteristic and is used to construct the CP-PFD [10]. In Fig. 5 the phase detector output of the PLL is grounded through a pull-down resistor and then connected to an operational amplifier in the voltage-follower mode for buffering. As a result, the three state characteristic of the mode-2 PD is converted to a two-state one. Therefore, the 4046's PD works as a MPD, while using the advantage of its sensitivity to phase error signs.

In this circuit the PLL center frequency is selected near the resonant frequency. However, at start-up the resonant frequency may be different than the center frequency of the PLL depending on the parameter changes. As a result, the PLL will spend a transient duration to track the resonant frequency at start-up. According to [10], the resonant inverter and the CP-PFD model were introduced using the linearization of the resonant tank phase curve near the resonant frequency.

In this paper, the authors use the linearization technique presented in [10] for a MPD and the transient behavior of these two PDs are compared with each other. For the CP-PFD the proposed circuit presented in [10] was implemented.

A block diagram of the PLL with the modeling of the parallel resonant tank is shown in Fig. 6, where Δf is the frequency deviation due to the mismatch between the center frequency of the PLL circuit and the resonant frequency at start-up, $t=0$. Δf_o is the instant difference between the switching frequency and the resonant frequency. Fig. 7 shows the phase of the parallel resonant impedance seen by the inverter with a quality factor of about 40. The LPF is the transfer function of the Loop Filter, which is the first-order RC low-pass filter presented in Fig. 5, K_{VCO} is the VCO's gain, and K_{PD} is the PD's gain.

K_β block is the slope of the resonant tank's phase respect to frequency at the resonant frequency where the phase of the resonant tank is zero; K_β is derived by linearizing the phase curve of the parallel resonant tank phase around the resonant frequency. K_β and the transfer function of a PLL with a resonant tank circuit are derived by equation (8) and

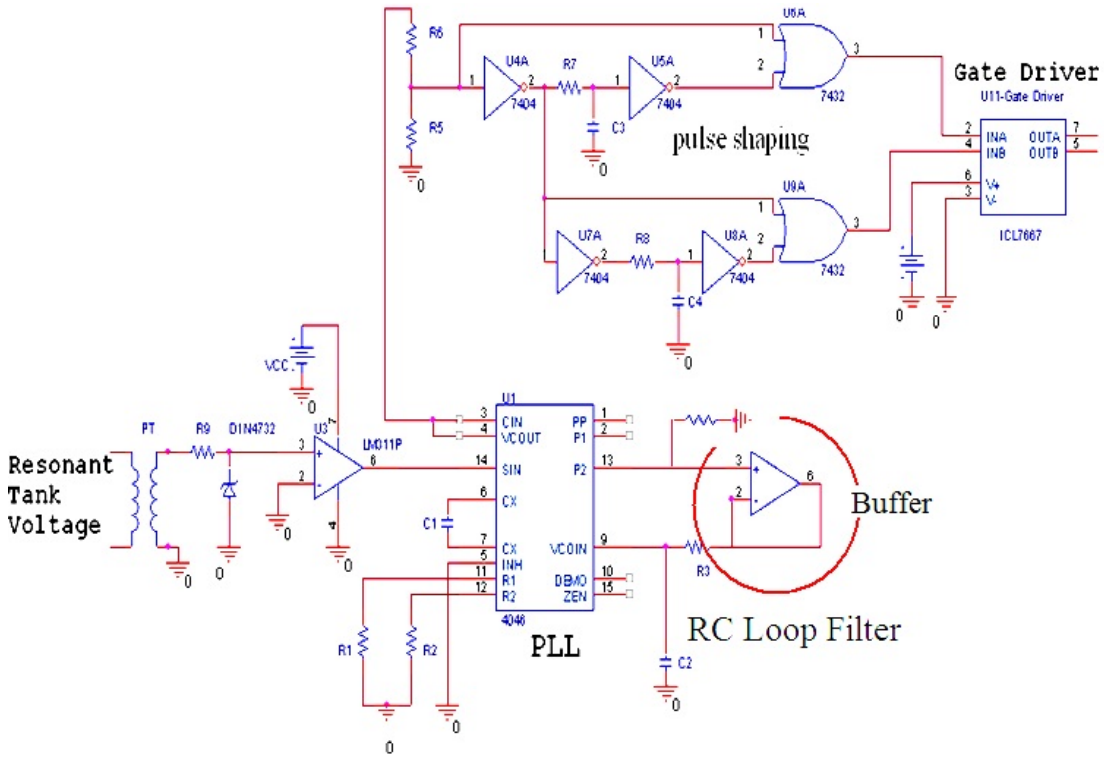

Fig. 5. The PLL circuit based on MPD and triggering circuits.

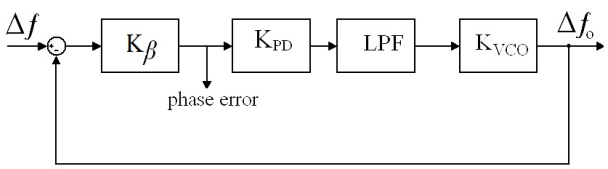

Fig. 6. Block diagram of PLL beside resonance inverter.

(9).

$$K_\beta = -\frac{\partial Z(j2\pi f)}{\partial f}|_{\omega=\omega_r} \tag{8}$$

$$G(S) = \frac{\Delta f_o}{\Delta f} = \frac{\frac{K_\beta K_{PD} K_{VCO}}{\tau}}{s + \frac{1+K_{PD}K_\beta K_{VCO}}{\tau}}, \tau = RC. \tag{9}$$

According to (10) the time constant of *G(s)* must be designed such that the PLL tracks the frequency faster than the dynamic response of the IH system while the phase error is negligible in the steady state condition. According to the HC/HCT4046A phase detector, the ripple at the output of the PD is two times the center frequency [16], [17]. To attenuate the ripples, the time constant of the LPF is designed with a cut-off frequency as follows, where the f_{center} is the PLL center frequency:

$$\tau = RC \leq \frac{f_{center}}{10}. \tag{10}$$

The steady state phase error of the PLL circuit is derived by equation (11) and according to Fig. 6.

$$\beta = \lim_{s\to 0}\left(S\left(\frac{K_\beta(\tau s+1)}{\tau s+1+K_\beta K_{PD}K_{VCO}}\right)\frac{\Delta f}{s}\right)$$
$$\beta = \frac{K_\beta \Delta f}{1+K_\beta K_{PD}K_{VCO}}. \tag{11}$$

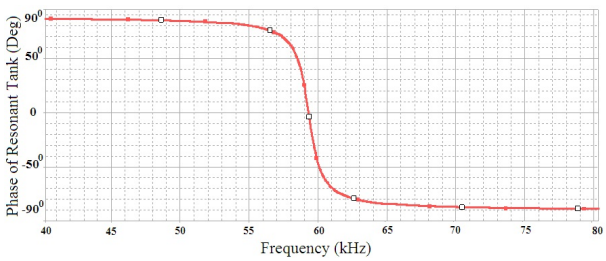

Fig. 7. Phase of the parallel resonant tank at no load condition.

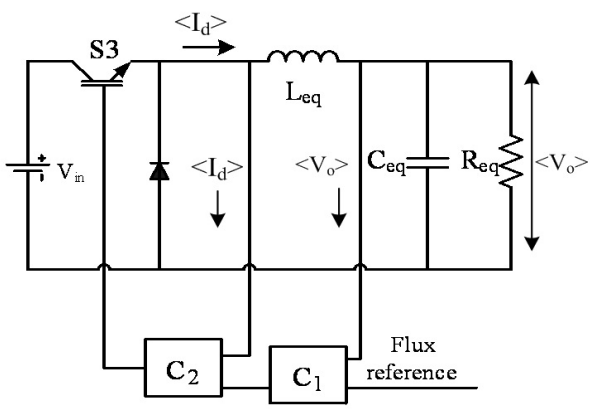

Fig. 8. Proposed cascaded coil flux control scheme.

According to the phase plot of the parallel resonant tank with the parameters presented in Table I, K_β is derived as follows:

$$K_\beta = -\frac{\partial Z(j2\pi f)}{\partial f}|_{\omega=\omega_r} \approx 0.704\,(rad/kHz)$$

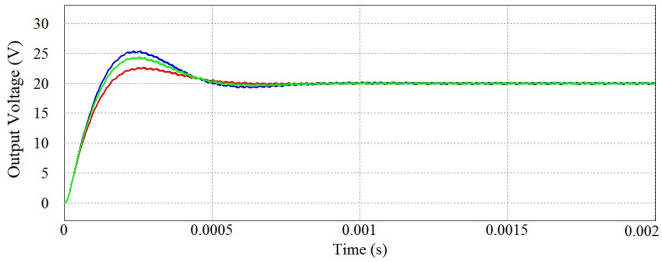

Fig. 9. Closed-loop step response of output voltage.

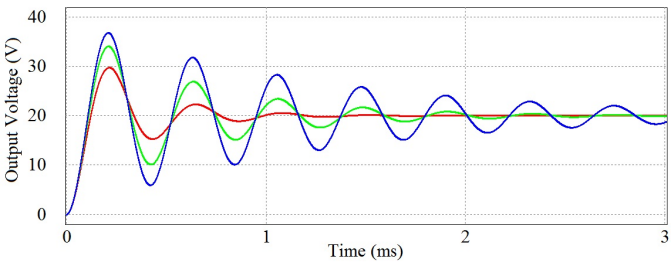

Fig. 10. Open-loop step response of output voltage.

According to the proposed phase detector of the 4046, K_{PD} and K_{VCO} are derived as follows:

$$K_{PD} = \frac{V_{DD}}{2\pi} \quad K_{VCO} = \frac{\Delta F}{V_{DD}}$$

where V_{DD} and ΔF are the supply voltage of the 4046 and the hold in the range frequency [16], [17]. According to equation (11) the steady phase error is derived as follows, when the hold in the range frequency is two times the center frequency, and the hold in the range of the PLL circuit is selected at its maximum value to attenuate β:

$$\beta = \frac{0.704\Delta f}{1+0.704\times\frac{V_{DD}}{2\pi}\frac{2\times 58.3}{V_{DD}}} \cong 0.050\Delta f = 2.88^0\Delta f(\text{Deg/kHz})$$

According to the calculated phase error, the frequency variation of the proposed IH system is assumed to be 2 kHz, which is adequate for the diamagnetic work-piece IH application due to the lower variation of the resonant frequency [2]. As a result, the maximum phase error will be 2.88^0 which is negligible.

IV. Control Method

In this paper the output current is controlled by adjusting the dc-link current I_d using a buck converter. The proposed cascaded coil flux control is shown in Fig. 8, and is based on the second-order average model of the CSPRPI presented in Fig. 4 and equation (4). As can be seen in Fig. 8, the dc-link current reference is produced by the output current in the cascaded scheme and the total model works as a buck converter. The output voltage is proportional to the output current of the work-coil. Therefore, the output voltage signal is used in the cascaded scheme and hence, the coil flux is

TABLE I
Resonant Tank Specifications

C_r	1.2μF
L_r	6μH
Q	40
f_r	58 kHz

TABLE II
Controller's Specifications

P_1, I_1, and D_1	2.5, 2.5e4, 2e10-4
P_2	8.5
Outer loop feedback gain	0.1
Inner loop feedback gain	1

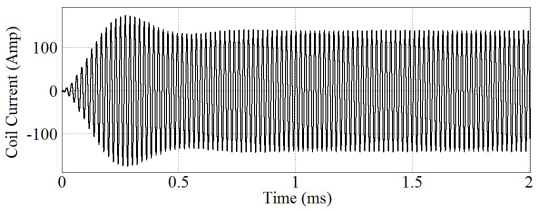

Fig. 11. Step response of coil current under cascaded coil flux control.

controlled. The relationship between the output voltage and the coil flux is shown by equation (12) where λ_o is the output flux. According to the average model, the simulation results for the output voltage and the output current control based on Fig. 8 will be the envelop of original signals. $<I_d>$ and $<V_o>$ represent the average model of original signals according to the buck model of the CSPRPI [11].

$$\lambda_o \propto \hat{I}_o \approx \frac{\hat{V}_0}{\omega_r L_r} \quad \text{for } Q >> 1. \tag{12}$$

There are two compensators, C_2 and C_1. The latter is the coil flux compensator and the former serves as the dc-link current controller.

The inner loop must have a fast dynamic for short circuit protection. Therefore, C_2 should be a proportional compensator. C_1 is a PID controller to compensate the dynamic response of the resonant inverter at start-up even in the worst case. The worst case occurs when the quality factor of the resonant tank is at its maximum value or when the inverter works under the no-load condition. To derive the parameters of C_1 and C_2 the average model of the inverter is used along with the buck converter. To show the validity of the proposed control method, a simulation is done where C_r, L_r, $L_{1,2}$, and Q are 1.2μF, 6μH, 1000μH, and 40, respectively. The parameters of the compensators namely C_1, C_2, and the feedback gains, as seen in Table II, are derived using a Genetic Algorithm (GA) to optimize the step response output voltage [18].

Utilization of such evolutionary algorithms for the sake of control parameters optimization has been widely addressed in many works such as [19]. I, P, and D are the integrator, the proportional, and the differentiator gains for the C_1 and C_2 compensators.

Fig. 9 and Fig. 10 show the proposed closed-loop and open-loop step responses of the output voltage for values of R_e equal to 50, 20, and 10 ohms based on the PSIM simulator while using the average model presented in Fig. 8. In Fig. 9 the controllers' parameters are implemented by using the specifications obtained in Table II. According to the average model technique, envelop of the coil voltage will be proportional to the output voltage of the buck converter model. Fig. 11 shows the coil current under the cascaded coil flux control method.

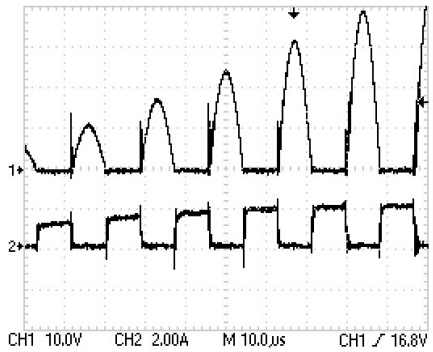

Fig. 12. Dynamic ZVS achievement of PLL based on MPD.

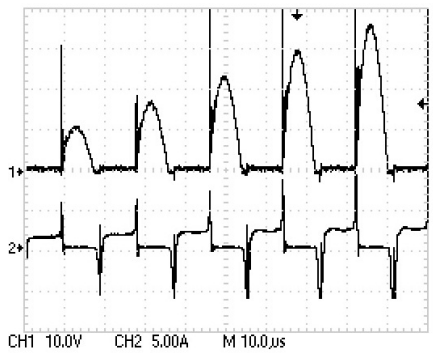

Fig. 13. Malfunction of PLL cricuit based on CP-PFD at start-up.

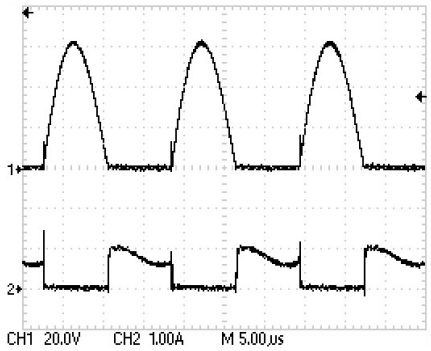

Fig. 14. Steady state operation of PLL circuit based on MPD.

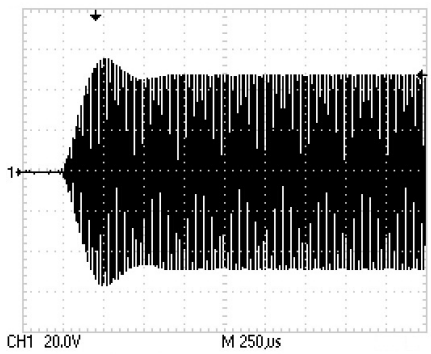

Fig. 15. Step response of coil voltage under proposed control.

V. Experimental Results

A laboratory prototype IH system was implemented to verify the validity of the proposed CSPRPI with the cascaded coil flux control method and the PLL circuit. The parameters of the CSPRPI are designed according to the considerations presented in previous sections. In this section the authors have designed the controller parameters and the PLL circuit parameters based on the resonant tank parameters presented in Table III.

Q_{nl} is quality factor of the resonant tank at the no load condition. The parameters of the PLL circuit, the compensators and the resonant tank are based on the formulations and values derived in previous sections. The frequency of the buck converter is selected as 30 kHz which is low in comparison to the resonant frequency, while the voltage ripple of the coil voltage is less than 5%.

Fig. 12 and Fig. 13 show the dynamic performance of the PLL circuit based on a MPD and a CP-PFD, respectively. As can be seen from Fig. 12 and Fig. 13, the dynamic performance of the proposed MPD is much better than that of the CP-PFD method. A switching failure definitely occurs if the CSPRPI uses the CP-PFD method for tuning without blocking diodes. In addition, the malfunction of the CP-PFD causes a high EMI in the start-up state due to hard switching performance. Fig. 13 shows the steady state performance of the PLL circuit based on a MPD close to the resonant frequency. The appropriate frequency change of the MPD is about 2 kHz near the center frequency of 58 kHz as derived in section III. The PLL specifications are listed in Table IV. According to Table IV and equation (10), the time constant of the PLL circuit is derived as follows, which is very short in comparison to the inverter dynamic response presented in Fig. 9 through Fig. 11:

$$\tau_{PLL} = \frac{\tau}{1 + K_{PD} K_{\beta} K_{VCO}} \simeq 15\mu s$$

Fig. 14 shows the ZVZCS performance of the voltage and current of the power MOSFETs at the steady state condition. Fig. 15 and Fig. 16 show the output voltage of the coil under the close loop and open loop conditions, respectively. The parameters of the compensators are implemented based on the simulation results in section IV. Fig. 17 shows the laboratory prototype with the PLL circuit, the buck converter, and the CSPRI.

TABLE III
CSPRPI Parameters

C_r	1.2μF
L_r	6μH
Q_{nl}	40
$L_{1,2}$	1000μH
S_1, S_2, *and* S_3	IRFP250
V_{in}	50

VI. Conclusion

This work presents a simple control technique for current source parallel resonant push-pull inverters for IH applications.

TABLE IV
CSPRPI Parameters

τ	200μs
f_{center}	58 kHz
Phase Detector	MPD
V_{DD}	12 V
ΔF	116 kHz

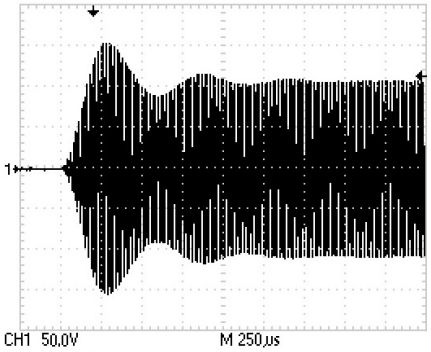

Fig. 16. Step response of coil voltage under open loop condition.

Fig. 17. The laboratory prototype.

It is shown that the cascaded coil flux control method has a better response to output parameter variations and that it works in a wide range of output power regulation. The advantage of this control method is its simple structure in comparison with adaptive and robust controllers. In this paper, to achieve dynamic ZVS at the start-up condition a PLL circuit is used based on the MFD method. The CSPRPI topology with this control method has a small package size and precise output power control for IH applications.

REFERENCES

[1] J. K. Byun, K. Choi, H. S. Roh, and S. Y. Hahn, "Optimal design procedure for a practical induction heating cooker," *IEEE Trans. Magn.,* Vol. 36, No. 4, pp. 1390-1393, Jul. 2000.

[2] V. Rudnev, D. Loveless, and R. Cook, *Handbook of Induction Heating*, Mracel Dekker, chap. 3, 2003.

[3] A. P. Hu, G. A. Covic, and J. T. Boys, "Direct ZVS start-up of a current-fed resonant inverter," *IEEE Trans. Power Electron.,* Vol. 21, No. 3, pp. 809-812, May 2006.

[4] A. L. Shenkman, B. Axelord, and V. Chudnovsky, "A new simplified model of the dynamics of the current-fed parallel resonant inverter," *IEEE Trans. Ind. Electron.,* Vol. 47, No. 2, pp. 282-286, Apr. 2000.

[5] P. Dawson and P. Jain, "A comparison of load commutated inverter systems for induction heating and melting applications," *IEEE Trans. Power Electron.,* Vol. 6, No. 3, pp. 430-441, Jul. 1991.

[6] R. Bonert and D. Lavers, "Simple starting scheme for a parallel resonance inverter for induction heating," *IEEE Trans. Power Electron.,* Vol. 9, No. 3, pp. 281-287, May 1997.

[7] A. Hirofumi, S. Takeshi, and N. Akira, "130 kHz 7.5Kw current source inverter using static induction transistors for induction heating applications," *IEEE Trans. Power Electron.,* Vol. 3, No. 3, pp. 303-309, Jul. 1988.

[8] N. J. Park, D. Y. Lee, and D. S. Hyun, "A power-control scheme with constant switching frequency in class-D inverter for induction-heating jar application," *IEEE Trans. Ind. Electron.,* Vol. 54, No. 3, pp. 1252-1260, Jun. 2007.

[9] A. R. Namadmalan, J. S. Moghani, and B. Abdi, "Improved modification of the current source parallel resonant push-pull inverter for induction heating applications," *International Review of Electrical Engineering,* Vol. 5 No. 2, pp. 390-396, Apr. 2010.

[10] H. Karaca and S. Kılın?, "Nonlinear modeling and analysis of resonant inverter tuning loops with voltage-pump phase-frequency detector," *IEEE Trans. Power Electron.*, Vol. 20, No. 5, pp. 1100-1108, Sep. 2005.

[11] T. J. Liang, R. Y. Chen, and J. F. Chen, "Current-fed parallel-resonant DC–AC inverter for cold-cathode fluorescent lamps with zero-current switching," *IEEE Trans. Power Electron.,* Vol. 23, No. 4, pp. 2206-2210, Jul. 2008.

[12] Z. Wu, J. Zhao, and J. Zhang, "Cascade PID control of buck-boost-type DC/DC power converters," in *proceedings of the 6th World Congress on Intelligent Control and Automation,* Jun. 2006.

[13] A. R Namadmalan, B. Abdi, and J. S. Moghani, "Current-fed parallel resonant push-pull inverter with coil flux control for induction heating applications," *in proceeding of Power Electronic & Drive Systems & Technologies Conference*, Feb. 2010.

[14] M. K. Kazimierczuk and A. Abdulkarim, "Current Source parallel-resonant DC-DC converter," *IEEE Trans. Ind. Electron.,* Vol. 42, No. 2, pp. 199-208, Apr. 1995.

[15] A. W. Green, "Modeling a push-pull parallel resonant convertor using generalized state space averaging," *IEE Proceedings-B*, Vol. 140, No. 6, pp. 350-356, Nov. 1993.

[16] G. C. Hsieh, and J. C. Hung, "Phase lock loop techniques-a survey," *IEEE Trans. Industrial Electron.,* Vol. 43, No. 6, pp. 609-615 , Dec. 1997.

[17] CMOS Phase-Locked-Loop Applications Using the CD54/74HC/HCT4046A and CD54/74HC/HCT7046A, *Texas Instrument,* September. 2002.

[18] S. M. R. Rafiei, A. Amirahmadi, and G. Griva, "Chaos rejection and optimal dynamic response for boost converter using SPEA multi-objective optimization approach," *in proceeding of IECON,* pp.3315-3322, 2009.

[19] E. Elbeltagi, T. Hegazy, and D. Grierson, "Comparison among five evolutionary-based optimization algorithms," *Advanced Engineering Informatics,* Vol. 19, No.1, pp. 43-53, Jan. 2005.

Alireza Namadmalan was born in Ahvaz, Iran, in 1987. He received his B.S. from the Isfahan University of Technology (IUT), in 2009. He received his M.S. in Electrical Engineering from the Amirkabir University of Technology, in 2011, and is currently pursuing his Ph.D. His research interests include induction heating, resonant converters, switching power supplies, electrical machines and drives, and high frequency transformers.

Javad Shokrollahi Moghani was born in Tabriz, Iran, in 1956. He received his B.S. and M.S. in Electrical Engineering from the South Bank Polytechnic and the Loughborough University of Technology, England, in 1982 and 1984, respectively. From 1984 to 1991 he was with the Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran. He received his Ph.D. in Electrical Engineering from Bath University, Bath, England, in 1995. After graduating he returned to the Amirkabir University of Technology where he has been ever since. His research interests include electromagnetic system modeling and design using FEM, DC-DC converters and electric drives.

Jafar Milimonfared received his B.S. in Electrical Engineering from the Amirkabir University of Technology, Tehran, Iran, and his M.S. and Ph.D. from Paris VI University, Paris, France, in 1981 and 1984, respectively. He joined the Amirkabir University of Technology as an Assistant Professor in 1984, where he is now a Professor of electrical engineering. From 1990 to 1993 and from 1997 to 2005, he was the Deputy of the Ministry of Science, Research and Technology in Iran. He is now the Head of Iran Mechatronics Society and the Head of Iran's Society of Morality in Science and Technology. His research interests include electrical machine design and analysis, power electronic and variable speed drives.