A new high speed and low power four-quadrant CMOS analog multiplier in current mode

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Abstract

In this paper a new CMOS current-mode four-quadrant analog multiplier and divider circuit based on squarer circuit is proposed. The dual translinear loop is the basic building block in realization scheme. Supply voltage is 3.3 V. The major advantages of this multiplier are high speed, low power, high linearity and less dc offset error. The circuit is designed and simulated using HSPICE simulator by level 49 parameters (BSIM3v3) in 0.35 µm standard CMOS technology. The simulation results of analog multiplier demonstrate a linearity error of 1.1%, a THD of 0.97% in 1 MHz, a $-3\,\text{dB}$ bandwidth of 41.8 MHz and a maximum power consumption of 0.34 mW.

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1. Introduction

The four-quadrant multiplier is a very important building block of analog signal processing system. It has many applications in automatic gain controlling, phase locked loop, modulation, detection, frequency translation, square rooting of signals, neural networks and fuzzy integrated systems. At present, the power consumption is a key parameter in the design of high-performance mixed-signal integrated circuit. Moreover, linearity and the accuracy parameters are very important in the analog multiplier design.

The multiplier performs the product of two continuous signals $x$ and $y$, yielding an output $z = Kxy$, where $K$ is a constant with suitable dimension. The linearity, speed, supply voltage and power dissipation are the main goals of design. Specific structures or topologies for the analog multiplier that have high speed, low-power dissipation and good linearity are designed. CMOS technology is widely recognized as the most desirable technology for integrated circuits implementation [1]. In multiplier circuit presented in [2], two supply voltages $V_{DD}$ and $V_{SS}$ are required, and also nonlinearity error is considerable. In the other circuit introduced by Tanno et al. [3] linearity is good but the power consumption is high. The multiplier circuits presented in [4–7] are not very good for low-voltage and low-power applications. Several techniques for reducing power consumption in CMOS analog multiplier circuits have recently been proposed. They use floating gate MOS [8–10], bulk-driven MOS [11], subthreshold mode [12,13] or class-AB mode [14,15]. They suffer for not being highly precise and not having low power and high speed. However, these analog multiplier circuits have been proposed using multiplication either in voltage or in current form.

In this paper, we present a low-power, high-speed four-quadrant analog multiplier circuit in current mode using “dual translinear loops”, where it works with a supply
voltage of $V_{DD}=3.3$ V. The circuit is based on the square-law characteristics of an MOS transistor operated in the saturation region. In addition, the dual translinear loops allow the design of the analog multiplier circuit, which exhibits wide bandwidth, high dynamic range and high speed [16,17].

2. Circuit description

2.1. Current-mode squarer circuit

Fig. 1 shows the current-mode squarer circuit based on the dual translinear loop. We will use this circuit to realize the multiplier circuit. The circuit consists of a dual translinear loop ($M_1$–$M_4$). The drain-to-source current ($I_{DS}$) of an MOS transistor operated in the saturation region is given by

$$I_{DS} = K(V_{GS} - V_t)^2$$  \(1\)

$$V_{GS} = V_t + \sqrt{\frac{I_{DS}}{K}}$$  \(2\)

where $K = 0.5\mu_0C_{ox}(W/L)$ is transconductance parameter of transistor, $\mu_0$ is the electron mobility, $C_{ox}$ is the gate oxide capacitance per unit area, $W/L$ is the transistor aspect ratio, $V_{GS}$ is the gate-to-source voltages and $V_t$ is threshold voltage of the MOS transistor. Consider a loop of MOS transistor $M_1$–$M_4$; summing the gate–source voltages around the loop gives

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4}$$  \(3\)

Transistors $M_1$–$M_4$ form a dual translinear loop in Fig. 1. They are biased in saturation region and are well matched and have the same transconductance value, that is $K_N = K_P$. Then using (1) and (2) and considering $I_{DS1} = I_{DS2} = I_B$, we have

$$\sqrt{I_{DS1}} + \sqrt{I_{DS2}} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}}$$  \(4\)

$$2\sqrt{I_B} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}}$$  \(5\)

Writing KCL at nodes A and B

$$I_{DS3} = I_{out} + I_{in}$$  \(6\)

$$I_{DS4} = I_{out} - I_{in}$$  \(7\)

Fig. 1. Proposed current squaring circuit.

Fig. 2. Simulation result of proposed current squaring circuit and error measurement (frequency = 500KHz).
Substituting (6) and (7) in (5) and squaring both sides

\[4I_B = I_{in} + I_{out} - I_{in} + 2\sqrt{I_{out}^2 - I_{in}^2}\] (8)

Eliminating \(I_{in}\) and squaring both sides again

\[16I_B^2 - 16I_B I_{out} + 4I_{out}^2 = 4I_{out}^2 - 4I_{in}^2\] (9)

The output current \(I_{out}\) of the circuit in Fig. 1 can be written as

\[I_{out} = \frac{I_{in}^2}{4I_B} + I_B\] (10)

As we can see (10) is the current squarer of the input signal, and simulation result of it is shown in Fig. 2.

2.2. Multiplier circuit

The principle of operation of the proposed multiplier is based on the square-difference identity:

\[(X + Y)^2 - (X - Y)^2 = 4XY\] (11)

The proposed analog multiplier circuit is shown in Fig. 3. It is based on the squaring circuit of Fig. 1 and two dual translinear loops. The first loop (\(M_1-M_4\) provides a \((X + Y)\) input function to the squarer function \((X + Y)^2\) and the second loop (\(M_5-M_8\) provides a \((X - Y)\) input function to the squarer function \((X - Y)^2\)

\[I_{o1} = \frac{(I_X + I_Y)^2}{4I_B} + I_B\] (12)

\[I_{o2} = \frac{(I_X - I_Y)^2}{4I_B} + I_B\] (13)

\[I_{out} = I_{o1} - I_{o2}\] (14)

Substituting (12) and (13) into (14) results in

\[I_{out} = \frac{I_X I_Y}{I_B}\] (15)

Thus, It is clearly seen that (15) yields the multiplication between \(I_X\) and \(I_Y\) and the division by \(I_B\) (\(I_B\) is a constant equal to 10 \(\mu\)A). The analog multiplier circuit of Fig. 3 is simulated using HSPICE with level 49 model (BSIM3v3) of 0.35 \(\mu\)m CMOS technology, and the supply voltage is 3.3 V, \(I_B\) is set to 10 \(\mu\)A and output port is connected to \(V_{DD}/2\).

Fig. 4 shows the dc transfer characteristics of the proposed multiplier, from which it can be deduced that the multiplier
has high linearity. Fig. 5 shows the other simulation results with error measurement in which the inputs are sinusoidal at 1 MHz which yields the sinusoidal output with high precision. Simulation results show the linearity error of 1.1%.

The total harmonic distortion (THD) versus input current signal at 100 KHz and 1 MHz are also shown in Fig. 6.

2.3. The divider circuit

Rearranging \( (15) \), we obtain

\[
I_{\text{out}} = \frac{I_X I_Y}{I_B}
\]  

(16)

Thus, by keeping the current \( I_X \) (or \( I_Y \)) constant, the output current of the circuit of Fig. 3 will be proportional to \( I_Y/I_B \) (or \( I_X/I_B \)) and the divider circuit can be obtained. However, care must be taken as \( I_B \) cannot be reduced below a minimum value in order to guarantee the proper biasing of the transistors. Simulation result of the divider circuit is shown in Fig. 7.

3. Performance analysis

In this section, the characteristics of analog multiplier of Fig. 3 will be analyzed. Input range, input and output impedance, mismatched and body effect error are discussed.

3.1. Error due to body effect

In an MOS transistor, as the source-to-substrate voltage \( V_{SB} \) increases, the threshold voltage \( V_t \) will also increase. This is the “body effect”, which can be characterized by

\[
V_t = V_{t0} + \gamma \left[ \sqrt{2\phi_b + |V_{SB}|} - \sqrt{2\phi_b} \right]
\]

(17)

where \( V_{t0} \) is the zero-bias threshold voltage, \( \gamma \) is the body-effect coefficient and \( \phi_b \) is the bulk potential. To avoid this effect, the cascaded MOS transistors are placed in separated wells, and \( V_{SB} \) will be zero. Thus, these transistors will have zero-bias threshold voltage. In \( M_2 \) and \( M_4 \) transistors bulk is connected to the source, hence \( V_{SB} = 0 \) and \( V_t = V_{t0} \), but in
Fig. 7. Simulation result of the divider circuit.

$M_1$ and $M_3$ transistors $V_{SB} \neq 0$. Considering this mismatch between $M_1$ and $M_3$ transistors we can write

$$V_{GS1} = V_{t1} + \Delta V_1$$

$$V_{GS3} = V_{t3} + \Delta V_3$$

Substituting (18) and (19) in (3) yields

$$V_{t1} + \Delta V_1 + V_{GS2} = V_{t3} + \Delta V_3 + V_{GS4}$$

where $V_{t1} = V_1 + \delta$, $V_{t3} = V_1 - \delta$, and $\delta$ is the mismatch term between $V_{t1}$, $V_{t3}$.

Rewriting Eq. (5), $I_{DS1} = I_{DS2} = I_B$, $I_{DS3} = I_{DS4} = I_{out} - I_{in}$ and assuming $V_{t2} = V_{t4}$ ($|V_{SB}| = 0$) we obtain

$$\delta + 2 \sqrt{\frac{I_B}{K}} = -\delta + \sqrt{\frac{I_{out}^2 + I_{in}}{K}} + \sqrt{\frac{I_{out}^2 - I_{in}}{K}}$$

Squaring both sides twice and ignoring the terms containing $\delta^2$, the current $I_{out}$ can be expressed as

$$I_{out}' = \frac{I_{in}^2}{4I_B + 8\delta \sqrt{KIB}} + \frac{I_B + 4\delta \sqrt{KIB}}{1 + 2\delta \sqrt{KIB}}$$

Assuming $I_B = K\Delta V^2$

$$I_{out}' = \frac{I_{in}^2}{4K\Delta V(\Delta V + 2\delta)} + \frac{K\Delta V(4\delta)}{1 + 2\delta / \Delta V}$$

In this equation we can see that the mismatch error between threshold voltages is dispensable. Because $\Delta V \gg 4\delta$, $\Delta V \gg 2\delta$, $1 \gg 2\delta / \Delta V$.

Subtracting (14) from (23) we obtain output current error quantity

$$|I_{error}| = |I_{out} - I_{out}'| = \frac{I_{in}^2}{4K\Delta V^2} + K\Delta V$$

$$- \frac{I_{in}^2}{4K\Delta V(\Delta V + 2\delta)} + \frac{K\Delta V(\Delta V + 4\delta)}{1 + 2\delta / \Delta V}$$

Ignoring terms containing $\Delta V^2 (n = 3, 4, 5)$, $\delta^2$

$$|I_{error}| = \frac{\delta}{2K\Delta V} I_{in}^2 + 4K\delta \Delta V^2$$

The term $\Delta V^2$ in (25) shows very small error. The advantage of using the function $(X + Y)^2 - (X - Y)^2$ in the multiplier circuit is to cancel the offset and body effect errors by eliminating the second term in (22). Consequently the output current will be given by

$$I_{out} = \frac{I_X I_Y}{I_B + 2\delta K \Delta V}$$

3.2. Input range and I/O resistance

The input current range of the multiplier is restricted by dual translinear loop, $M_1 - M_4$ and $M_5 - M_8$, operating in saturation region. If we assume that the MOS transistors $M_1 - M_4$ operate in saturation region, we can write (4) or (5).
Substituting (6) and (7) in (5) and squaring both sides

\[ 2\sqrt{I_B} \geq \sqrt{I_{out} + I_{in}} + \sqrt{I_{out} - I_{in}} \]  

(27)

Assuming \( I_{in} = X I_B \) and substituting (10) in (27), we obtain \( X \) or namely maximum current value with which the multiplier circuit can work correctly

\[ 2\sqrt{I_B} \geq \sqrt{\frac{X^2 I_B^2}{4} + I_B + X I_B} + \sqrt{\frac{X^2 I_B^2}{4} + I_B} - X I_B \]  

(28)

Squaring both sides and eliminating \( I_B \) we obtain \( X = 0 \), or \( X = \pm 2 \), where \( X = +2 \) is acceptable: \( I_{in} \leq 2 I_B \).

In the multiplier circuit, maximum input current is: \( I_{in_{max}} = I_X + I_Y \). Therefore \( I_{in} \) will be maximum if

\[ |I_X| = |I_Y| \leq |I_B| \]  

(29)

Assuming input ports are SUM and SUB, and output port is SUB, the input and output impedances are

\[ R_{in_{SUM}} = r_{ds7}(1 + g_{m7} r_{ds8})||r_{ds10}(1 + g_{m10} r_{ds12}) \]  

(30)

\[ R_{in_{SUB}} = r_{ds1}(1 + g_{m1} r_{ds2})||r_{ds9}(1 + g_{m9} r_{ds11}) \]  

(31)

\[ R_{out} = r_{ds7}(1 + g_{m7} r_{ds8})||r_{ds10}(1 + g_{m10} r_{ds12}) \]  

(32)

Fig. 8 shows the layout of the current-mode analog multiplier circuit, in which metal 1 was only used.

4. Conclusion

A four-quadrant CMOS multiplier based on the new squaring circuit was proposed. The performance of the multiplier was simulated using HSPICE software. The advantages of the proposed analog multiplier circuit over previous circuits are high speed, high bandwidth and low-power consumption. Comparison between the proposed multiplier and the two previously reported multipliers are shown in Table 1.

The multiplier can be used in analog VLSI circuit for low-power and high-speed applications such as IF variable gain amplifiers, adaptive filters, phase locked loops, neural networks and integrated fuzzy systems.

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<thead>
<tr>
<th></th>
<th>[2]</th>
<th>[4]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption (mW)</td>
<td>0.46</td>
<td>0.055</td>
<td>0.34</td>
</tr>
<tr>
<td>Bias current (μA)</td>
<td>10</td>
<td>0.25</td>
<td>10</td>
</tr>
<tr>
<td>Power supply (V)</td>
<td>±1.5</td>
<td>2</td>
<td>3.3</td>
</tr>
<tr>
<td>THD (%) (1 MHz, 20 μA)</td>
<td>3.7</td>
<td>1 (1 KHz)</td>
<td>0.97</td>
</tr>
<tr>
<td>Nonlinearity (%)</td>
<td>1.20</td>
<td>5</td>
<td>1.1</td>
</tr>
<tr>
<td>−3 db bandwidth (MHz)</td>
<td>19</td>
<td>0.2</td>
<td>41.8</td>
</tr>
<tr>
<td>Technology (μm)</td>
<td>0.5</td>
<td>0.35</td>
<td>0.35</td>
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</tbody>
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 References


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