Assessing Testing Techniques for Resistive-Open Defects in Nanometer CMOS Adders

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Abstract— As we move to smaller CMOS technologies, the need for better testing techniques arises. We investigate the effectiveness of four testing techniques against resistive-open defects. The tests are applied to two adder topologies, namely the quasi-clocked adder and the bridge-style adder. The tests are done under full process variations for technologies down to 16nm. The test techniques based on dynamic power supply current (iDDT) show superiority for large-feature technologies, but as the technology decreases delay tests appear to be the most effective.

Keywords- nanometer technologies; process variations; iDDT; Wavelet; delay test; adders

I. INTRODUCTION

As the industry shifts its technology deep into the nano-scale, the complexity and sophistication of the implemented designs continues to advance. Since the costs of manufacturing at nanometer technologies are dropping it is not economically feasible to tolerate the increasing cost for testing. Nanometer technologies are characterized by vulnerability to new process defects and higher process variability. The current fault models do not effectively represent all the faults in nanometer technologies, and thus traditional testing techniques are not fully effective [13].

One class of defects in nanometer technologies is modeled as resistive-open defects. This model is hard to detect using traditional testing techniques. Such techniques include voltage testing and IDDQ testing [15,16]. IDDQ techniques are becoming ineffective because nanometer technologies in CMOS circuits are characterized by high leakage current. Thus researchers are investigating different testing methodologies through exploiting the transient current at the power supply and ground rails. Thus the detection of abnormal behavior of transient current is used to detect a fault. iDDT testing [17-24] is used in static CMOS circuits and it continues to prove effective with decreasing technology sizes. However we aim to investigate the effectiveness of iDDT for future CMOS circuits down to 16nm, for that we test several variants of iDDT testing that include the wavelet transform. In this work, we take into account the large process variations associated with nanometer technologies and we use technology parameters based on the Predictive Technology Model (PTM) [9]. Moreover, we investigate the effectiveness of delay tests because some resistive-open defects do not affect the correctness of the output of a circuit but it introduces a significant delay at the output.

The rest of this paper is organized as follows: in section 2 we discuss the related work. In section 3 we describe process variations. In section 4 we present the testing techniques used. In section 5 we present the experimental setup; then in section 6, we show the simulation results. Finally, we conclude in section 7.

II. RELATED WORK

Several researchers tackled the issue of digital circuit testing in nanometer technologies. The most prevalent techniques are iDDT testing, and delay testing under large process variations.

Choi et al. proposed in [3] a sizing algorithm to stabilize the speed of the circuit under process variations with a certain degree of confidence keeping the power and area within a limited budget. The algorithm estimates the circuit delay variations based on statistical timing analysis conducted on the process variations, and then re-sizes the circuit to obtain the desired yield.

Min et al. presented in [7] a formal method to identify faults that could be tested by iDDT and generated relevant input vectors to detect them using the Boolean process. The testing method is based on the average value of iDDT from the input vector change until the circuit reaches steady state. Moreover, the authors of [5] proposed a new iDDT method to detect open defects and delay faults based on the variation of the transient power supply current. The tests showed that some open defects lead to a delay behavior and this causes a variation in the iDDT waveform as well.

Lu et al. proposed in [6] an advanced way to detect the smallest local delay faults under process variations by finding the longest path, which can detect the smallest local delay faults caused by an open defect. Franco et al. proposed in [11] a new way to test for the delay faults in digital circuits. The main idea is to analyze the output waveform between the samples of the clock to understand the circuit delay. This method is most suitable when high fault coverage of the delay faults is required, and when the test invalidation becomes a major concern due to a dynamic hazard. Hence, two classes of output analysis are proposed: pre-sampling and post-sampling analysis. Post-sampling analysis observes the output for any
change in the output value after the sample time to insure stability, while pre-sampling analysis collects output data before the sample time and compares between the faulty and fault-free results to detect delay faults.

The authors in [8] describe a parallel fault simulator which detects faults by comparing the resulting delay to a pre-computed delay for the good circuit. The first function of the simulator is thus computing the actual timing to be used in the delay test, which takes into consideration product specifications as well as the tester’s accuracy in initiating transitions. The second function is a 6-step parallel fault simulation procedure that determines fault coverage (Setup conditions, Dry run, Slack calculation, Selection of possible Faults for simulation, Fault simulation, and Diagnostic data generation). Each delay fault is represented by a block of the circuit with transition delay that exceeds the manufacturer’s specification. For this, the simulator takes as input the actual timings computed in step 1 and a list of faults to be tested.

In [1,2] the authors introduce a scheme for fault detection and localization using the wavelet transform of iDDT waveform. Then, localization is applied using delay measurement techniques. This method was applied to two circuits based on 0.25μm TSMC technology with random input stimuli. The results obtained showed that this method is resistant to iDDT waveform changes and that the wavelet based method is superior to other techniques.

III. PROCESS VARIATIONS

Different transistors have different parameters even though they might have similar nominal values specified during the manufacturing process. These variations appear as WID (within-die), D2D (die to die) and W2W (wafer-to-wafer). There are many reasons for process variations such as implant impurity levels, substrate, poly-silicon and changes in dielectric thickness [10]. In fact, the stability of parameters is affected by the modernity of the used technology. As the technology scales the parameters become less stable, hence newer technologies have large process variations that may exceed ± 25% for some parameters. These discrepancies affect the reliability of the nominal values on which several design decisions are based. Moreover, these variations affect the reliability of chip testing because they affect the measures used by these tests for distinguishing the defect-free chips from defective ones. For example, the reliability of one of the main measures used in chip testing, the peak and average power supply or ground currents, is deteriorated by process variations. Hence it is essential to consider all possible variations in the CUT when assessing the effectiveness of a certain testing method.

IV. DETECTION METHODS

In this work we consider four detection methods for resistive-open defects. The first test is based on measuring the peak value of iDDT when we switch the circuit under full process variations, and then we compare the different values for defective and defect-free circuits. The second test is the normalized RMS of the continuous wavelet transform (CWT) of iDDT, where we compare the value to a given threshold. The third test is the RMS of CWT of iDDT where we compare the RMS of the defect and defect-free circuits. The last test is the delay test where we measure the time it takes for the primary outputs to settle from the time we switch the primary inputs. For the three iDDT-based methods, the currents taken into account are the ground and power supply currents. When the defect is located in the pull-up network, we consider the power supply current and when the defect is in the pull-down network, we consider the ground current. Moreover, we generate the input test vector that excites the circuit branch containing the defect.

V. EXPERIMENTAL SETUP

We performed simulations for a 3-bit ripple carry adder configuration, where a fault was introduced to a 1-bit block at a time. In the setup, we placed two inverters at each input and fanout buffers at the outputs. We also considered two different adder topologies, the quasi-clocked adder and the bridge-style adder. We considered 20 faults in the quasi-clocked which we collapsed to 6 faults, and for the bridge-style adder we considered 52 faults which we collapsed to 12 faults, as shown in Figures 1 and 2.

We performed the experiments for four nanotechnologies: 45nm, 32nm, 22nm and 16 nm. The value of a resistive open used depends on the technology and it increases for decreasing technologies. The process parameters are based on PTM and the process variations are introduced on the channel length (L), width (W), oxide thickness (Tox), threshold $V_t$ and $V_{DD}$ according to a normal distribution where the standard deviations are based on ITRS and are shown in Table I.

![Figure 1 Defect positions of 1-bit quasi-clocked adder circuit](image-url)
VI. RESULTS

We performed fault simulations of the selected adders using Monte Carlo analysis in HSpice with complete process variations. Below are the results for the logic level test, $I_{DDT}$ tests and delay test.

A. Quasi-Clocked Adder

1) Logic Level Test

The first test we applied when we introduced the faults is the logic level test which is used to verify the functionality of the CUT in case the faults altered the functionality of the circuit. The results of the Monte Carlo analysis for this test were not conclusive as the best fault coverage obtained was 10% and the worst coverage was 0%. Obviously, this method is not effective for the detection of resistive open defects.

2) $I_{DDT}$ Tests

Three tests were conducted for the transient current when the circuit is switched. Those include the peak magnitudes of the current, RMS wavelet and normalized RMS wavelet.

   a) Peak current magnitude

   We generated the distribution of peak $I_{DDT}$ currents with each fault introduced, and compared them to the defect-free distribution. We obtained three different patterns for the distributions: Complete overlap, partial overlap and no overlap. An example with no overlap is shown in Figure 3 for Fault 2 at 22nm. The $x$-axis in Figure 3 is peak current in Amps.

   In Figure 4 we show the complete fault coverage of the different tests. A test is considered effective only when there is no overlap in the distributions. We can see that as the technology decreases the effectiveness of the peak current test decreases from 100% in the 45nm technology to 0% in 16nm. Thus peak current is suitable for large-feature technologies but it is not suitable for the futuristic 16nm technology, and hence we need to rely on other testing techniques.

   b) RMS Wavelet

   In these tests we plotted the distribution of the RMS of the wavelet transform of the transient current for the faulty circuit and compared it to the defect-free distribution. We obtained similar patterns of overlap as the peak current test, but with a slightly higher coverage. Nevertheless, the RMS Wavelet test has 0% coverage for 16nm technology.

   c) Normalized RMS Wavelet

   We computed the normalized RMS wavelet and used a threshold of 10%. This test was effective for all technologies in the case of the quasi-clocked adder.

3) Delay Test

The propagation delay of the adder was measured and the distributions for the defective and detect-free circuits were plotted. In the cases of 45nm, 32nm and 22nm we obtained 100% fault coverage, however, we obtained 50% coverage for
the 16nm technology. This is smaller than the coverage of the normalized RMS wavelet test.

B. Bridge-Style Adder

Figure 5 shows the fault coverage of all four tests for the different technologies. In the case of the bridge-style adder we obtained similar results compared to the quasi-clocked adder: the peak current test effectiveness decreased when the technology decreased, the performance of delay test was superior to other tests in the 45nm, 32nm and 22nm, and the normalized RMS wavelet test was the most effective in the 16nm technology.

Figure 3 Bridge-style adder fault coverage for different tests and technologies

VII. CONCLUSIONS AND FUTURE WORK

In this paper we evaluated the effectiveness of different testing techniques based on 1dmax and delay. The tests evaluated are the delay test, peak current magnitude test, RMS wavelet test and the normalized RMS wavelet test. The tests were performed for two adder topologies, the quasi-clocked adder and bridge-style adder. We generated the collapsed the fault set and the corresponding test vectors that excite the CUT branch with the open resistive defects. The results showed that under full process variations, the most effective testing techniques were the delay test and the normalized RMS wavelet test. As a future work we can test other adder topologies and increase the number of bits in the adder inputs, which may cause more switching in the circuit and thus mask the effect of a fault. Such a problem can be addressed using clustering techniques by dividing the circuit into smaller blocks, at the expense of overhead in the separate power supplies and ground rails needed for the each cluster.

REFERENCES


