Guest Editors’ Introduction: Special Section on Chips and Architectures for Emerging Technologies and Applications

Alfredo Benso, Senior Member, IEEE, Yiorgos Makris, Senior Member, IEEE, and Pinaki Mazumder, Fellow, IEEE

It is with great pleasure that we introduce this special section on Chips and Architectures for Emerging Technologies and Applications to the audience of the IEEE Transactions on Computers.

We are currently witnessing a technology advancement which is making the gap between the present and future much narrower than it has ever been. The purpose of this special section is to showcase highly innovative, creative, and futuristic chip architectures and functionalities that can range from new paradigms in reconfigurable systems architectures, to adaptive, organic, ubiquitous, and biologically inspired computing, to new classes of chip implants, or any other highly innovative human-to-computer interface.

This special section includes two papers, which we hope will offer an interesting perspective on the challenges involved in designing integrated circuits and architectures that leverage the capabilities of emerging technologies in novel applications.

The first paper, “Exploring the Potential of Threshold Logic for Cryptography-Related Operations,” by Alessandro Cilardo, investigates the application of a non-Boolean computational paradigm to cryptographic applications. More specifically, the author demonstrates the power of linear Threshold Logic functions, which are enabled by new technologies such as Resonant Tunneling Diodes (RTDs), Single-Electron Tunneling (SET), Quantum Cellular Automata (QCA), and Tunneling Phase Logic (TPL), towards performing fundamental cryptographic operations. An architecture for implementing such operations, namely a Montgomery modular reduction and multiplication, is also introduced and its intrinsic superiority to traditional Boolean computational models in demonstrated.

The second paper, “3D Integration of CMOL Structures for FPGA Applications,” by Z. Abid, Ming Liu, and Wei Wang, introduces a combination of hybrid CMOS/nanoelectronic (CMOL) circuits and 3D integration, in order to develop a 3D CMOL technology with particular emphasis on designing Field-Programmable Gate-Array (FPGA) chips. The authors discuss the architecture, 3D integration, defect tolerance and performance aspects of this technology, as well as its breakthrough potential for developing the next generation of FPGAs.

We would like to thank the previous editor-in-chief of the IEEE Transactions on Computers, Dr. Fabrizio Lombardi, for suggesting that we organize this special section, the current editor-in-chief Dr. Albert Y. Zomaya, for hosting this section, and all of the editorial staff for the support in the making of the issue. Additionally, we would like to thank the authors of the submitted papers and the numerous reviewers whose contributions made this special section possible.

Alfredo Benso
Yiorgos Makris
Pinaki Mazumder
Guest Editors

A. Benso is with the Department of Computer Engineering, Politecnico di Torino, Torino, Italy. E-mail: alfredo.benso@polito.it.
Y. Makris is with the Departments of Electrical Engineering and Computer Science, Yale University, New Haven, CT 06520-8267, USA. E-mail: yiorgos.makris@yale.edu.
P. Mazumder is with the Department of Electrical Engineering and Computer Science, University of Michigan at Ann Arbor, Ann Arbor, MI 48109-2121, USA. E-mail: mazum@eecs.umich.edu.

For information on obtaining reprints of this paper, please send e-mail to: tc@computer.org.
Alfredo Benso received the MS in Computer Engineering and the PhD in Information Technologies, both from Politecnico di Torino. He currently holds a tenured associate professor position in computer engineering at Politecnico di Torino, Italy. His research interests include fault tolerance estimation, memory testing, microprocessor testing, and hardware architectures and software pattern recognition techniques for bioinformatics. He is also actively involved in the Computer Society, where he has been the leading volunteer for several projects. He is a Computer Society Golden Core Member, and a senior member IEEE.

Yiorgos Makris received the Diploma of computer engineering and informatics from the University of Patras, Greece, in 1995, and the MS and PhD degrees in computer science and engineering from the University of California, San Diego, in 1997 and 2001, respectively. He is currently an associate professor of electrical engineering and computer science at Yale University, where he leads the Testable and Reliable Architectures (TRELA) Research Group. His current research interests include soft-error mitigation in digital circuits, machine learning-based testing of analog/RF circuits, mitigation of hardware Trojans, as well as test and reliability of asynchronous circuits. He serves on the organizing and program committees of many conferences in the areas of test and reliability and is the program chair for the 2011 Test Technology Education Program (TTEP) of the IEEE Test Technology Technical Council (TTTC). He is a senior member of the IEEE.

Pinaki Mazumder received the PhD from the University of Illinois at Urbana-Champaign in 1988. He is a professor of electrical engineering and computer science at the University of Michigan (UM). During 2007 and 2009, he was on leave for three years from the UM to serve as the lead program director of the Emerging Models and Technologies Program at the US National Science Foundation. For six years he worked in industrial R&D centers that included AT&T Bell Laboratories, where in 1985 he started the CONES project - the first C modeling based VLSI synthesis tool, and India’s premiere electronics company, Bharat Electronics Ltd., where he developed several high-speed and high-voltage analog integrated circuits intended for consumer electronics products. He has published over 250 technical papers and four books on various aspects of VLSI research works. His research interest includes current problems in Nanoscale CMOS VLSI design, CAD tools and circuit designs for emerging technologies including Quantum MOS and resonant tunneling devices, semiconductor memory systems, and physical synthesis of VLSI chips. Dr. Mazumder was a recipient of the Digital’s Incentives for Excellence Award, BF Goodrich National Collegiate Invention Award, and DARPA Research Excellence Award. Dr. Mazumder is an AAAS Fellow (2007) and an IEEE fellow (1999) for his contributions to the field of VLSI.

For more information on this or any other computing topic, please visit our Digital Library at www.computer.org/publications/dlib.