Reliability aspects of gate oxide under ESD pulse stress

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A B S T R A C T

Power law time-to-breakdown voltage acceleration is investigated down to ultra-thin oxides (1.1 nm) in the ESD regime in inversion and accumulation. Breakdown modes, oxide degradation and device drifts under ESD-like stress are discussed as function of the oxide thickness. The consequent impacts on the ESD design window are presented.

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1. Introduction

For ESD protection design in advanced CMOS technologies, thin gate oxide (GOX) vulnerability to over-voltage is strongly reducing the ESD design window. A precise knowledge of the GOX breakdown voltage, the possible degradation, and impact of surges caused by ESD on the GOX lifetime (time to dielectric breakdown, TDDB) is necessary for ESD designers. In this work, we show experimental results on gate oxides with physical thicknesses in the range of 1.1–16 nm.

The first part of this work will demonstrate the TDDB power law validity even down to 1.1 nm for high performance CMOS. Furthermore, a thorough investigation of inversion and accumulation biasing mode for NFET and PFET allows identifying NFET/inversion as the most critical configuration for ESD. Then in a second part, GOX post breakdown modes in the EOS and ESD domains will be described and the ultra-thin pFET soft breakdown mode will be discussed. The third part of this contribution focuses on device degradations under non-destructive ESD stress, which has not been well studied for oxides in the direct tunneling EOT range up to now. The drift behavior of devices is different for thin and thick gate oxides, which is related to the different charge trapping behavior. In both cases, the impact of moderate ESD-like stress on hot carrier device lifetime is exposed. In the last section, a discussion on the failure criteria including dielectric and device degradation is developed for defining a safe-ESD design window. Finally, a review on GOX breakdown, degradation and impacts for ESD design is summarized. All oxide thicknesses considered in the paper correspond to physical thickness values.

2. Thin gate oxide time-to-breakdown voltage acceleration

It was found that the TDDB voltage acceleration of thin gate oxides in the ESD range can be described by the same power law as used for lifetime extrapolation [1]. This observation is also true for oxide thickness down to 1.1 nm as shown in Fig. 1, which plots the voltage acceleration behavior over 10 orders of magnitude. The constant voltage stresses (CVS) measurements were performed in inversion and accumulation biasing mode at room temperature for a minimum of 35 samples per voltage level. The stresses were done using the same configuration, set-up and measurement techniques described in [1]. Small active GOX structures with optimized layout in terms of minimizing parasitic resistance effects have been used. In contrast to the 1.5 nm gate oxide nFET, no increase in voltage acceleration around 4 V has been observed for the 1.1 nm gate oxide nFET. Therefore, this voltage acceleration increase, which leads to a critical ESD robustness issue, is not a general trend for thinner oxides.

The general oxide voltage acceleration behavior of nFETs stressed in inversion at room temperature for seven distinct thicknesses is summarized for the same normalized area in Fig. 2. For both regimes, above or below the universal change in the TDDB voltage acceleration factor [2] which is occurring around 5 V for nFET devices, power laws with a common exponent accurately fit the data. Regardless of the technology and thickness, the same acceleration factor can be used. In this case, a voltage acceleration of 48 provides a good fit for the nFET data in inversion below the kink and a lower acceleration of 30 is found above it. From this general behavior, the effective time-to-breakdown scaling factor as a function of the physical oxide thickness can be extracted. The TDDB dependence of the oxide thickness is consistent with the percolation cell model [3]. A TDDB oxide thickness scaling factor around six decades in time per nanometer is found for...
In meaningful statistical failure level (see Section 5). We are close to the
ent for other areas and is also dependent of the choice of a mean-
type. The GOX breakdown as a function of oxide thickness is differ-
voltage acceleration is dependent on the stress polarity and device
mulation and inversion stress. It should be mentioned that this
thickness is plotted in Fig. 4 for NMOS and PMOS devices in accu-
and should be carefully considered.

inversion, the main focus in this part, is the most critical case
and optimized ESD protection concepts. It is shown that nFET in
the device and regime choices for the ESD-safe design of thin buffer
capacitors [4]. The ESD robustness hierarchy of nFET and pFET with
the stress polarity can then be deduced and allows the
characterization data, GOX breakdown voltage values in the ESD
and EOS time domains for oxide thicknesses in the range of
6.85–1.1 nm stressed in inversion at room temperature can be
extrapolated.

ESD events can lead to a stress in accumulation, for example in
buffer capacitors. Thus, the same characterization work was done
in accumulation biasing mode and has revealed different voltage
acceleration power law compared to the inversion biasing mode
(a comparative example is given for the 1.1 nm nFET in Fig. 1). This
has a direct impact on the robustness against over-voltages and
should be considered for the ESD design guidelines. This affects
the device and regime choices for the ESD-safe design of thin buffer capacitors [4]. The ESD robustness hierarchy of nFET and pFET with respect to the stress polarity can then be deduced and allows the identification of an ESD weakness for the choice of appropriate and optimized ESD protection concepts. It is shown that nFET in inversion, the main focus in this part, is the most critical case and should be carefully considered.

The GOX breakdown in the HBM regime as a function of oxide thickness is becoming crucial for the design of ESD robust ICs.

3. Gate oxide post breakdown modes

As previously shown, the time-to-breakdown is following the
same acceleration law as a function of the stressing voltage between the long and medium term reliability and the ESD time range. However, a difference can be seen in the gate oxide’s post breakdown modes, which can be soft or progressively increasing in conductivity until being hard. The time resolution of the measurement set-up as well as device type, stress polarity, and active GOX area play a role in experimentally evaluating the different modes [5]. Contrarily to long and medium DC time range (EOS) in case of 100-ns pulses, not the first soft breakdown is detected but oxide is stressed into a harder breakdown mode. A typical Scanning Electron Microscopy (SEM) failure analysis picture for a hard breakdown is shown in Fig. 5.

TDDB tests performed on nFETs for oxide thickness down to 1.1 nm allow a good data matching between the ESD and the long/medium time domains, because there is no significant difference in time between soft and hard breakdown observed in these experiments. For the 1.1 nm pFET stressed in the inversion biasing mode, a difference is measured between the long/medium time

Fig. 1. Voltage acceleration for 1.1 nm nFET and pFET stressed at room temperature obtained from conventional TDDB and short-time measurements set-ups.

Fig. 2. Voltage acceleration of nFET stressed in inversion for seven oxide thicknesses (6.85–1.1 nm).

Fig. 3. TDDB cross section from Fig. 2 at 4 V showing the acceleration factor from the GOX time-to-fail as a function of the oxide thickness.

Fig. 4. Breakdown voltage acceleration as a function of the physical oxide thickness for nFET and pFET stressed at 25 °C in the HBM range of time for a normalized size of 1.2 μm².
and the ESD range (Fig. 6), because the time difference between soft and hard breakdown becomes remarkable long. The use of the first breakdown event as a failure criterion in the DC range leads to a severe mismatch with the data obtained in the nanoseconds regime whereas the consistent use of the hard breakdown criterion in the DC range results in a perfect data correlation. This is an experimental artifact, which needs to be considered to correctly interpret the data and to avoid wrong conclusions for the ESD design window. The same is true for pFET in accumulation biasing mode. The progressive increase in the gate leakage is shown in Fig. 7a and b; it demonstrates how clearly soft breakdown in the progressive phase and a hard breakdown can be experimentally distinguished for pFET. The power law characteristic of post breakdown gate leakage [6] can be used for identifying the post breakdown mode as:

\[ I_g = a \times V_B^b \]  

(1)

Hard breakdown results in an ohmic characteristic, which means \( b = 1 \). Values larger than one indicate that the post breakdown mode is in the progressive phase. The larger the value of \( b \), the closer is the status of the breakdown spot to the initial percolation path which forms the first SBD.

In the case of pFET triggering on soft breakdown becomes a delicate task for TDDB tests in the ESD range, because during the applied voltage pulse, a low voltage drop on linear scale is caused by a small current increase on logarithmic scale, which itself already represents the progressive phase. In addition to this experimental problem in accumulation biasing mode the well resistance may cause a voltage drop during high voltage breakdown tests in the ESD time range. In Fig. 8a the \( I_g-V_g \) characteristic of gate leakage reveals a resistance of \( 1 \, \text{k}\). This allows correcting measured time-to-breakdown (Fig. 8b) and plotting the real difference in time between medium and ESD test range as discussed above.

GOX soft breakdown can cause GIDL in narrow transistors [7] and characteristic shifts but may not have damaged the IC functionality in some logic domains [8–10]. A net increase in the leakage gate current is seen and this event will be succeeded later on by a HBD after the residual time, which is independent of the pre-stress. For ESD robust and reliable designs, no GOX breakdown should be allowed and the ESD design window must be fixed with attention for sensitive pFET devices in accumulation configuration. However, in most of the cases the ESD design window limit is given by the worst-case of nFET biased in inversion. In a general manner, the conservative approach allows also in worst-case, a possible extended reliability margin due to the SBD mode. As the nature of the gate oxide breakdown is a statistical phenomenon, this margin should not be used to enable low GOX failure rate.

4. Gate oxide damage under non-destructive ESD-like pulse stress

In this paragraph, the degradation of the dielectric and its impact on the device integrity will be discussed as a function of the oxide thickness. The degradation nature of the gate oxide is cumulative and the question arises, what would be the impact of non-destructive ESD stress on a device? A lot of work has already been done in that field for thick oxides [11–16], but there is very little work on thin oxides below 3 nm [17–20]. To answer this question, positive rectangular pulse stresses (100 ns) were applied to nFET gate transistors with drain, source and bulk grounded (capacitors in inversion). The tests were performed on a wide range of oxide thicknesses.

4.1. Thick oxide (>2.5 nm)

4.1.1. Oxide to device degradation induced by ESD-like stresses

One has to distinguish between thin oxide (<2.5 nm) and thick oxides. For thick oxides, it is possible to monitor a straight and clear influence of the ESD stress on device characteristics due to a strong trapping. The increase in the threshold voltage (Fig. 9a) is one example for such device degradation. This phenomenon begins at a stress level of around 70–80% of the characteristic breakdown voltage \( (V_{BD}) \) of the Weibull distribution of VRS. The shifts right after the stress can be sufficient to drift transistor characteristics out of specifications and possibly lead to a failure. For example, a 10% change in the saturated threshold voltage is considered a fail. The damage mechanisms originate from interface traps generation and charge trapping in the oxide bulk. Uniform interface trap generation has been evidenced by charge pumping measurements done on a 5.2 nm thick oxide (Fig. 9b). Concerning the trapped carriers in the bulk oxide, this can be directly observed (Fig. 10) in the Stress Induced Leakage Current (SILC) [21,22]. The oxide degradation under short 100-ns pulses shows the increase in the gate leakage current (SILC) followed by an abrupt hard post breakdown state. The modeling of the post breakdown leakage curves in Fig. 10 uses Eq. (1).

A special focus has been put on the SILC generation in 2.65 nm nFET through CVS stress in the DC (10 ms) and in the ESD time domain (100 ns and 20 ns). The trap generation rate under DC or short pulses shows the same kinetic behavior (Fig. 11). The com-
mon power law relationship of the SILC generation [22–24] as a function of the injected charge is also valid in the ESD time range. This confirms the continuity of degradation mechanisms from DC until the 100 ns time range which has already been observed in TDDB measurements. During an ESD stress, there is less injected charges than during a DC stress (\(Q_{inj} = J_g \times C_s t_{stress}\)). The current density during an ESD stress (100 ns) is about 2–3 orders in magnitude higher than for a DC stress (10 ms), but the stress time is five orders in magnitude lower. This emphasizes that at high field, the SILC generation is not fluence-driven but rather voltage-dependent. The efficiency of the defects generated by the injected charge is consequently increasing with voltage. This matches the gate-oxide degradation picture based on the release of the maximum energy from injected carriers at the anode side [3,25,26]. The SILC generation is dependent on the injection procedure [24,27,28], the pulse stress width and the temperature dependence on the SILC generation rate have been reported in the ESD time regime in [17]. Above all, it was concluded with high statistical certainty in [23] that no reliable correlation exists between the critical amount of SILC at breakdown and the critical defect density at breakdown.

![Image](Fig. 7) (a) Progressive increase in the monitored gate leakage current of 1.1 nm pFET stressed in accumulation by Voltage Ramp Stress (VRS). (b) Post breakdown gate leakage of a 1.5 nm pFET device stressed in accumulation with CVS.

![Image](Fig. 8) (a) 1.1 nm pFET \(I_g - V_g\) characteristic obtained from DC and short pulse measurement. The fitting of the tunneling current reveals internal devices voltage drops. (b) Voltage acceleration for 1.1 nm pFET stressed in accumulation obtained from conventional TDDB and VRS short-time measurements.
However, the SILC is still a good indicator of the oxide deterioration induced by ESD stresses as its significant occurrence (Fig. 12a) is coming together with DC characteristic drifts (Fig. 9a) around 80% of $V_{BD}$.

Carriers trapped in the bulk oxide or near the interface responsible of device characteristic drifts and SILC could be de-trapped with time or annealed at high temperature [29]. In the relaxation process observed at room temperature, two different time constants are revealed (Fig. 12b). Initially, the superficial traps are de-trapped in a very short time ($\sim 10$ s) and then the deep level traps further into the oxide are relaxing much more slowly. Trapping and relaxation capability are linked to the oxide quality and the processing steps (as the nitridation for example); thus recovery effects are technology and/or device dependent.

### 4.1.2. Possible latent damage induced by ESD

For long term device reliability topic, I/O nFETs (5.2 nm) were investigated. The degradation of nFETs just after a 100 ns inversion mode stress at 90% of $V_{BD}$ first results in a strong positive trapping (accompanied also with negative traps) as seen in DC characteristic drifts. Then, after one hot carrier (HC) stress cycle or after some minutes these positive charges relax or get neutralized, leaving a net negative charge in a quite stable state. This degradation behavior can be observed in Fig. 13 in the saturated drain current ($I_{dsat}$) and in the saturated transconductance ($g_m$). A similar first unstable positive trapping behavior has been observed for 3.2 nm nFET stressed in inversion under TLP stress [17]. The injection of this large amount of carriers resulting from the ESD stress could induce an acceleration of the device degradation. This can be revealed by
post electrical stress [11–13]. To evaluate the impact of a moderate ESD stress on the device lifetime, hot carrier (HC) stresses at the maximal substrate current condition (worst HC stress for thick oxide) were performed on pre-pulsed devices. The post HC stresses were performed about 10 min after the stress only at the point where device characteristics have reached the second stable phase (Fig. 13, state 2). The ESD-like stress and the HC stress seem to be purely cumulative; the HC kinetic degradation of stressed devices is slightly lower as fresh ones but shifted by a strong initial trapping which is dependent on the pre-stress level (Fig. 14). At long term, the charges generated by the ESD stress are merged in the high quantity of carriers generated by the HC stress. No reduction in the device lifetime is noted for ESD-like pre-stress up to 85% of $V_{BD}$. On the other hand, the strong trapping induced by a stress within 90% of $V_{BD}$ leads to a clear effect on the device lifetime.

To fully evaluate the impact on the device lifetime, HC stresses were performed at different stressing drain voltage on fresh and pre-stressed devices at a fixed value of 90% of $V_{BD}$ (Fig. 15). The ESD stressed devices have the lifetime reduced by a factor 15 (Fig. 16). As device degradation due to a moderate uniform ESD stress applied to the gate is purely dependent on the ESD stress level (in relation to the amount of trapped charges, see Fig. 14), the question is if these stressed devices can be annealed by charges detrapping, leading to the partial recovery of the device reliability cri-

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**Fig. 11.** SILC generation under CVS injection with various pulse width stresses. From DC to high and short pulse stresses the kinetic of the SILC hold the same power law behavior.

**Fig. 12.** (a) SILC generation as a function of the percentage of the breakdown voltage ($V_{BD}$) for a 5.2 nm nFET. (b) Characteristic recovery effect in time at room temperature from stressed devices by a 100 ns pulse stress.

**Fig. 13.** Saturated drain current from an 5.2 nm nFET after an 100 ns pulse stress at 90% of the breakdown voltage. In a first step (1) a threshold voltage ($V_t$) reduction due to unstable positive charges occurs, then in a second phase (2) the degraded characteristic is dominated by a net negative trapping (increased $V_t$ and $I_{on}$ reduction).
Tox: 5.2 nm
nFET
L: 0.24 μm
W: 25 μm

Fig. 14. Impact of the ESD pre-stress level on the hot carrier degradation kinetic. A pure cumulative effect of the charged induced from the ESD stress is revealed. No consequent long term lifetime impact is noticed for stress levels below 85% of the breakdown voltage.

Fig. 15. HC stresses at the maximal substrate current condition are applied on fresh and pre-stress devices at 90% of \( V_{BD} \). A clear impact on the hot carrier degradation kinetic can be observed.

Fig. 16. Hot carrier lifetime deduced from the Fig. 15. The pre-ESD stressed devices at 90% of \( V_{BD} \) have a reduced device lifetime of 1.5 decade in time.

4.2. Thin oxide (>2.5 nm)

In the case of thin gate oxides, it is more complex to understand the degradation because of carrier de-trapping by direct tunneling. Therefore, degradation in the bulk of oxide is not possible. Thin gate oxides are at least composed by two interface layers which can be degraded by the non-destructive ESD stress. In DC parameters the effect of the moderate stress is not very pronounced for the 2.2 nm and 1.5 nm nFET oxide tested. The stress can lead to some minor changes in parameters, smaller than 2% and very close to \( V_{BD} \) (Fig. 9a). The eventual interface traps generated under ESD pulse stress haven’t been observed in the gate current leakage via Low Voltage SILC [30,31]. In order to investigate the device lifetime degradation caused by moderate ESD stress, HC stresses have been performed after a moderate ESD-like pulse stress. Two different HC stress conditions have been performed, the worst case degradation for thin oxide which is occurring for the maximal field condition at \( V_G = V_D \) and the maximum substrate current bias condition. Hot carrier stresses after a 100 ns stress at 90% of the GOX breakdown value has minor impact on the HC degradation kinetic for the tested 2.2 nm oxide (Fig. 17). The weak trapping induced by the ESD stress is rapidly dominated by the HC degradation mechanisms and in the long term no HC lifetime criteria reduction has been noticed. Similar behavior was also observed for drain ESD stress configuration [19]. The ESD stresses and HC are purely cumulative, fewer amounts of defects generated or of charges trapped in thin oxide (no occupied volume traps due to the direct tunneling distance) does not lead to any specific device reliability issues. For an ESD stress in the range of 90% of \( V_{BD} \), no degradation could be monitored but the dielectric lifetime will be consequently affected [1] (see Section 5). A possible latent damage is seen here if the lifetime margin criteria fixed basically by the power law voltage acceleration is not taken into account.

5. Failure criteria selection for the ESD design window

Let’s define the GOX breakdown voltage \( V_{BD} \) as the value obtained for the 63% failure criteria and assume that over-voltage stresses dominates GOX dielectric lifetime with a pure cumulative process (at least to a first order). Based on the TDDB power voltage acceleration law, the calculated lifetime as a function of the stress level is shown in Fig. 18 for two typical acceleration values 48 and 30. A deduced safe margin of about 10–15% for \( V_{BD} \) should be considered to ensure no dielectric lifetime consumption. This margin is only attributed to the TDDB power law voltage acceleration.
but the choice of an appropriate margin for the ESD design window is also strongly dependent on the oxide thickness. The cumulative failure distribution of the GOX time-to-fail under CVS is described by the Weibull statistic. The linear shape of the distributions plotted in a Weibull plot is expressed with the parameter $b$, called Weibull slope. These Weibull slopes are getting shallower for thinner oxides, equivalent in a spreading of the cumulative failure distributions through time \[3\]. At one stress voltage level and for a fixed failure criterion, the reduction of the time-to-fail is increases with the reduction of the oxide thickness (Fig. 19). A reduction in the time-to-fail also means a reduction in the gate oxide voltage (Fig. 20a) and thus should be accounted for the ESD design (Fig. 20b). The reduced time-to-fail for thinner oxides, results in a faster shrinking of the ESD design window for thinner oxide if the same acceptable statistical failure criteria is kept.

In case of thick oxides, the starting point of device degradation (~80% $V_{BD}$, Figs. 9a, 12a and 13) or specified drifts limits could be preferred as limiting failure criterion to ensure the functionality of sensitive circuits. In that case, a safe voltage margin can be chosen to ensure a reliable ESD protection. Basically this safety margin can be obtained via a percentage of the GOX breakdown voltage. If we consider defining the upper limit of the ESD design window below 90% of $V_{BD}$, this limit dominates the failure criterion imposed by the statistical cumulative distributions (FC < 100 ppm) as reported in the Fig. 21 for the 5.2 nm oxide. This effect is due to the steep Weibull slopes of thick oxides, which enable to reach high statistical failure criteria without a large reduction of the ESD design window. For thick oxide a focus on the starting point of device degradation could be used as the failure parameter for robust design. In the correlation established between the failure criterion resulting from the statistical nature of the GOX breakdown and the percentage of the GOX breakdown value (Fig. 21), arbitrary area and temperature are taken into account. The appropriate conditions should be considered for the evaluation of the GOX breakdown voltage reference ($t_{63\%}$).

For thin oxides nFET which are stressed in inversion a careful definition of the failure criteria considering the statistical probability of failure should be accounted due to the very shallow Weibull slopes. Actually, for qualification of products the whole gate oxide susceptible to be stressed must be taken into account. Basically the whole gate oxide area possibly exposed to a voltage surge during...
an ESD event (capacitors between supplies and ground, input/output gate) has to be summed-up. Then an acceptable failure criterion accounting for the statistical probability of GOX failure and for the dielectric lifetime consumption should be fixed. From Fig. 21, an acceptable failure criterion of 1% is covering both effects. Then the number of stress applied on I/Os in respect with polarity and power domains must be accounted for the effective stressing time. From these correct extrapolations the safe-ESD design window can be deduced for the design of protection elements.

For the definition of the upper limit of the ESD design window, it appears that a percentage of $V_{BD}$ is a sufficient failure criterion for thick oxide whereas for thin oxide the statistical failure criterion should be carefully considered.

6. Summary

It was shown that the breakdown of thin GOX in the ESD range can be accurately described by power law behaviors even down to 1.1 nm oxides. GOX breakdown projection in the ESD regime towards the limit of SiO$_2$ (or SiO$_2$N) dielectric thickness is reported without any deviation. The accumulation data presented complete the GOX breakdown overview in the nanosecond domain. Identification of ESD worst-case (nFET in inversion) and precise devices ESD robustness hierarchy with respect to the stress polarity is provided quantitatively. The reported ESD post breakdown mode for small GOX area is always hard, except for thin pFET stressed in accumulation where soft breakdowns could occur. A stress within 10% of the breakdown voltage (obtained from t$_{63\%}$ criterion) could theoretically lead to a non negligible reduction of the lifetime of the dielectric and device.

Thick to medium oxides I/O transistors from sensitive pins configurations could suffer from malfunctions due to ESD induced charge trapping and/or defects creation if the protection concept is not well adapted. This could be monitored by an increase in the gate leakage current (SILC) and in DC parameters drifts. For thick oxides (>2.5 nm), the safety margin must even be extended to $\frac{1}{2}$ of $V_{BD}$ to consider this strong oxide trapping effect impact on the transistor characteristics. However, this extended margin is not a strong issue for thick oxides in general as the ESD design window is more relaxed for thick oxides and is supported also from the steeper cumulative failure distribution slopes.

In contrast, the shallower Weibull slopes from thin oxides result in a larger reduction of the ESD design window in respect with the...
maintaining an acceptable failure criterion level. In this framework, no special issue concerning device reliability has been noticed for thin oxides nFET under non-destructive short pulse stresses.

The ESD-safe design could be tuned as a function of the standard or sensitive circuits to protect. For this, the choice of a meaningful failure criterion and method including oxide and dielectric degradation mechanisms depend strongly on the oxide thickness. For the critical case of thin nFETs, to prevent from gate oxides breakdowns, the ESD design window should consider: (a) the whole sensitive gate oxide area from the IC must be considered, (b) an acceptable failure criteria accounting for the statistical failure distribution and for the dielectric lifetime consumption should be chosen, (c) the number of stresses per I/O (polarity, power domains) must be accounted for the effective stress time endured by same GOX domains during qualification.

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References