A low-voltage low-power CMOS fully differential linear transconductor with mobility reduction compensation

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**A R T I C L E   I N F O**

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**A B S T R A C T**

A highly linear fully differential CMOS transconductor architecture based on flipped voltage follower (FVF) is proposed. The linearity of the proposed architecture is improved by mobility reduction compensation technique. The simulated total harmonic distortion (THD) of the proposed transconductor with 0.4Vpp differential input is improved from −42 dB to −55 dB while operating from 1.0 V supply. As an example of the applications of the proposed transconductor, a 4th-order 5 MHz Butterworth Gm-C filter is presented. The filter has been designed and simulated in UMC 130 nm CMOS process. It achieves THD of −53 dB for 0.4Vpp differential input. It consumes 345 μW from 1.0 V single supply. Theoretical and simulated results are in good agreement.

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1. Introduction

The transconductor providing voltage to current conversion is a basic building block in analog signal processing circuits such as continuous-time filters and oscillators. The overall performance of these applications is limited by the performance of the transconductor. The main non-ideal characteristics of the transconductor are limited linear input range, limited output impedance, finite signal to noise ratio, and finite bandwidth. The linearity performance is an important issue in the transconductor design since it is used in an open loop configuration.

Linearization by attenuation is one of the techniques used to improve linearity; the input voltage is attenuated by a factor \( k \), and the transconductor deals with an attenuated version of the input signal. An example of this category is source degeneration [1]. The disadvantage of this technique is the higher current and larger aspect ratio for the same transconductance value and over-drive voltage of input transistors. Another example of this category is using floating gates where natural capacitive dividing for input signal is provided, but it is not suitable for high frequency applications because of capacitive coupling.

Another linearization technique is to operate the input transistors in triode region while keeping the drain-source voltage constant. The drain current will be linear with respect to the applied gate-source voltage [2] but this technique has limited transconductance value and smaller tuning range.

Another linearization technique is achieved by means of an algebraic sum of nonlinear terms (the quadratic \( I-V \) characteristics of a transistor) yielding ideally only a linear term. Fig. 1 illustrates the conceptual idea of this linearization technique, where VA is a constant DC bias voltage.

This category of linearization techniques rely on the ideal quadratic \( I-V \) characteristics of a transistor operating in the saturation region. In deep submicron process, with reduction in transistor dimensions, linearity based on MOS square law behavior becomes worse due to the appearance of short channel effects such as mobility degradation. Therefore, a highly linear transconductor should be designed taking short channel effects into consideration.

A final example of linearization techniques is using pseudo differential pair transconductor. It has better linearity performance than its fully differential counterpart; however it needs an extra circuit of common-mode feedforward to improve the common mode rejection ratio (CMRR) [3].

In this paper a highly linear fully differential CMOS transconductor architecture based on (FVF) is proposed. In Section 2 an expression for the nonlinearity term due to mobility reduction was driven. Enhancement of linearity using mobility reduction

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compensation technique is shown. The frequency compensation and noise analysis are also discussed. The common-mode feedback (CMFB) circuit is shown in Section 3. A 4th-order 5 MHz Butterworth Gm-C filter as an application of the proposed transconductor is presented in Section 4. The simulation results of the filter before and after layout are also shown.

2. Proposed transconductor architecture

A low-voltage low-power fully differential transconductor based on differential flipped voltage follower (DFVF) [4–6] is represented.

2.1. Transconductor based on (DFVF)

Fig. 2 shows the circuit implementation of a DFVF. It is a non-linear differential input transconductor, which has an output current defined by

$$I_{out} = \beta(V_{AB} + V_{OD1})^2$$

where $\beta = 0.5\mu C_{ox}(W/L)$ is the MOSFET's transconductance parameter, $V_{OD1} = \sqrt{1/\beta}$ is the over-drive voltage of M1, and $V_{AB} = V_A - V_B = V_{peak} \cos \omega t$.

Fig. 3 shows the class AB [7] linear transconductor realized by cross-coupling a pair of non-linear transconductors of Fig. 2. The differential output current based on saturated MOS square law is linearly dependent on the differential input voltage as follows:

$$I_{od} = I_{o1} - I_{o2} = 4V_{AB} \sqrt{\beta A}$$

$$G_m = \frac{I_{od}}{V_{AB}} = 4\sqrt{\beta A}$$

Considering mobility degradation in short channel devices, $I_{out}$ in Fig. 2 will be modified as follows:

$$I_{out} = \frac{\beta(V_{AB} + V_{OD1})^2}{1 + (\theta(V_{AB} + V_{OD1}))}$$

where $\theta = 1/E_C$, $E_C = V_{sat}/\mu$, $L$ is the device electrical channel length, $\mu$ is the low field mobility, $V_{sat}$ is the saturation carrier drift velocity, $E_C$ is the critical electric field. Note that the value of $\theta$ has been determined for the used technology by a best fit to the simulated device characteristics, to be $0.4V^{-1}$. Using Taylor series expansion the 3rd-order harmonic coefficient of $I_{out}$ is given by

$$a_{3,\text{sat}} = \frac{\beta V_{peak}^3}{(1 + \theta V_{OD1})^3} \left[-0.25\lambda + 0.5V_{OD1}^2 - 0.25V_{OD1}^2 \lambda^2\right]$$

where $\lambda = \theta/(1 + \theta V_{OD1})$. It can be also shown that the fundamental coefficient $a_1$ is given by

$$a_1 = \frac{\beta V_{peak}^2}{(1 + \theta V_{OD1})^2} \left[2V_{OD1} - \lambda V_{OD1}^2\right]$$

Therefore the 3rd-order harmonic distortion is given by

$$HD_3 = \left|\frac{a_3}{a_1}\right| = \frac{\theta V_{peak}^2}{4V_{OD1}(1 + \theta V_{OD1})^2(2 + \theta V_{OD1})}$$

Fig. 4 shows the simulated $HD_3$ versus peak voltage of the input signal. The results are in good agreement with the calculated values using Eq. (5).

2.2. Mobility reduction compensation

Two voltage-to-current converters with the same sign of the fundamental harmonic and opposite signs for the 3rd-order harmonic are provided in our proposed transconductor; therefore
the nonlinearity term of composite transconductor can be reduced [12].

The modified transconductor is shown in Fig. 5. It is based on the fact that transistors working in saturation and weak inversion regions have opposite signs for the 3rd-order harmonic coefficient. In Fig. 5, transistor M4 is forced to work in weak inversion by the source follower M5 and it is placed in parallel with the main input transistor M3 working in saturation region. The current added to $I_{\text{out}}$ due to drain current of parallel transistor M4 is given by

$$I_{\text{out,sub}} = I_o \left( \frac{W}{L} \right) \frac{\beta_{\text{sat}}}{\zeta} e^{V_{\text{SG4}} / V_T} \left( \frac{W}{L} \right) \right)$$  \quad (6)

$I_o$ is the reverse saturation current, $\zeta$ is weak inversion slope factor, and $V_T$ is the thermal voltage.

$$V_{\text{SG4}} = V_{AB} + \left( \frac{V_{OD1} - V_{OD5}}{C_0} \right)$$  \quad (7)

By Taylor series expansion of Eq. (6), the 3rd-order harmonic coefficient due to sub-threshold transistor M4 is calculated to be

$$a_{3,\text{sub}} = \frac{I_o V_{\text{Peak}}^3}{24(\zeta V_T)^3} \left( \frac{W}{L} \right)^4 \frac{V_{OD1} - V_{OD5}}{V_T}$$  \quad (8)

Since the transconductor output current is the combination of both currents of the saturated transistor and the weak inversion transistor, the non-linearity term can be reduced by choosing proper aspect ratio of M4 and M5 such that

$$a_{3,\text{sat}} = -a_{3,\text{sub}}$$  \quad (9)

2.3. Final proposed transconductor

The final proposed transconductor is shown in Fig. 6 with a level shifter to increase input range [8] (discussed in Section 2.4), compensation capacitor $C_c$ for stability (discussed in Section 2.5), mobility reduction compensation technique to improve linearity, and cascode transistors M6 to improve output impedance $R_{\text{out}}$. Table 2 summarizes the dimensions and bias currents for all transistors.

Fig. 7 shows the $THD$ of the proposed transconductor. It is dominated by $HD_3$ and as the width of the weak inversion transistor is increased, $HD_3$ decreases from $-42$ dB in case of no compensation to $-80$ dB. The $THD$ reaches a minimum and becomes dominated by $HD_5$ (when $a_{3,\text{sat}} = -a_{3,\text{sub}}$), afterwards $HD_3$ is increased again.

Fig. 8 shows $G_m$ of the proposed transconductor versus differential input DC voltage at different values of $W_4$ (width of the weak inversion transistor M4). It is observed that $G_m$ tend to be more linear with increasing width of the weak inversion transistor after which $a_{3,\text{sub}}$ will be larger than $a_{3,\text{sat}}$ and $HD_3$ will increase again.
2.4. Input range limitation

In Fig. 2 to maintain M2 in saturation, we must satisfy $V_{in,\text{max}} < V_{DD} - V_{GSO2} - V_{GS1}$, and to maintain M1 in saturation, we must satisfy $V_{in,\text{min}} > V_{DD} - V_{GSO2} - V_{th}$. Thus, the input range = $V_{in,\text{max}} - V_{in,\text{min}} = V_{th} - V_{DD}$.

In order to increase the input range, a level shifter with voltage $V_{LS}$ in the feedback loop path between G2 and D1 is used as shown in Fig. 9. This results in $V_{in,\text{min}} = V_{DD} - V_{GSO2} - V_{LS} - V_{th}$, and the input range $\approx 2V_{th}$.

In the current design, we choose the aspect ratio of transistor M5 such that $(V_{GSO1} - V_{GSO5}) = 0.5V_{th}$, thus the condition to maintain M4 in sub-threshold region, as shown in Eq. (7), is $|V_{AB}| < 0.5V_{th}$.

2.5. Frequency response and stability analysis

The proposed $G_m$ cell has a closed loop formed by shunt feedback of the FVF; the stability of this feedback loop is studied. In Fig. 10, the loop is opened at the gate of M2 and a test voltage $V_T$ is applied to calculate open loop gain $A_{ol} = V_o/V_T$. The open loop gain is given by

$$A_{ol} = -0.5g_{m2}R_y$$ (10)

where $R_y = r_h/g_{m1}r_0f_{R2}$ is the open loop resistance at node y, the factor 0.5 is due to the current of M2 is split between two identical parallel branches. The resistance at node x is given by

$$R_x = 0.5\frac{(1 + r_h/r_{m1})}{r_{m2}}$$

Since $R_x \gg R_y$, there is a dominant pole at node y, $\omega_{py} = 1/C_yR_y$, and a non-dominant pole at node x, $\omega_{px} = 1/C_xR_x$, where $C_y$ and $C_x$ are the parasitic capacitance at nodes y and x, respectively. The gain bandwidth product $GB$ is given by $GB = \omega_{py}A_{ol} = 0.5g_{m2}/C_y$.

In order to ensure enough phase margin $\omega_{px} > 2 \times GB$ must be
satisfied. For \( r_b \approx r_e (R_e \approx 1/g_m1) \), this condition leads to \( C_y/C_y < g_m1/g_m2 \). So compensation capacitor \( C_C \) in parallel with \( C_y \) is needed to ensure enough phase margin. However, this will reduce the bandwidth of the transconductor. The proposed stability compensation scheme is based on adding \( C_C \) in parallel with \( C_y \), as shown in Fig. 10. In this case the bandwidth of the transconductor is not sacrificed for stability considerations. The gain between nodes \( x \) and \( y \) can be expressed as \( A = +(1+g_m1r_{e1})r_{b1}/(r_{e1}+r_b) \), this leads to a negative capacitor (using Miller effect) at node \( x \) given by \( C_x = -(A C_C) \), which can be chosen to tune out the parasitic capacitance \( C_y \) and move \( \omega_{pe} \) to high frequencies. The non-dominant pole of \( G_m \) cell becomes \( \omega_{nd} \approx 0.5g_m2/(C_y+C_C) \), and the excess phase can be expressed as
\[
\Delta \phi \approx -\tan^{-1} \left( \frac{\omega}{\omega_{nd}} \right)
\]

Fig. 11 shows peaking in the \( G_m \) in case of no compensation. Compensation capacitor in parallel with \( C_y \) will result in reduced bandwidth, the proposed stability compensation results in 82% increase in the bandwidth from 347 MHz with \( C_C = 30 \) fF in parallel with \( C_y \) to 633 MHz with \( C_C = 10 \) fF in parallel with \( M1 \).

2.6. Noise performance

Referring to Fig. 6, the noise contribution of M2 is neglected since it is common-mode noise. Consider only thermal noise power the input referred noise power of transconductor is given by
\[
\frac{V_{in,n}}{I_A} = 16K T \left[ \frac{1}{g_m1} + 0.5 \frac{g_m2}{g_m1} + 0.5 \frac{g_m5}{g_m1} \right]
\]
where \( K \) is the Boltzman’s constant. Increasing \( g_m1 \) will reduce noise, this can be achieved for the same over-drive voltage of input transistors by increasing input transistors’ aspect ratio \((W/L)\) and drain current at the expense of less bandwidth (due to the increased parasitic capacitance) and more power consumption.

2.7. Tuning

The tuning circuit, shown in Fig. 6, results in \( I_A = \beta (V_{GDD}+V_{CD})^2 \). Since \( G_m = 4 \sqrt{\beta I_A} \), then the overall transconductance can be given by
\[
G_m = 4 \beta (V_{GDD}+V_{CD}) = G_{mos} \left( 1 + \frac{V_{CD}}{V_{GDD}} \right)
\]

Thus the proposed transconductor can be linearly controlled by an external voltage \( V_{CP} \). For \( V_{CD} = \pm 0.5 V_{GDD} \), \( G_m \) can vary from 0.5\( G_{mos} \) to 1.5\( G_{mos} \), as shown in Fig. 12.

2.8. Mismatch errors

Due to the mismatch errors in \( V_{bo} \) and \( W/L \), a nonlinear 2nd order harmonic distortion \((HD_2)\) will appear in \( I_A \) as the differential output current. For \( \beta = 0.5 \mu m C_{mos} (W/L) \), assuming a mismatch factor \( \xi \) in the dimensions of the input transistors M3, resulting in a \( HD_2 \) in the output differential current obtained by replacing \( \beta \) by \( \beta \xi (1+\xi) \) in the current Eq. (1) of one of the two transistors. The \( HD_2 \) is given by
\[
HD_2 = \frac{\xi V_{peak}}{8 V_{GDD}}
\]

Table 1

Comparison with previously reported works.

<table>
<thead>
<tr>
<th></th>
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</tr>
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<tbody>
<tr>
<td>Technology</td>
<td>CMOS</td>
<td>0.5 ( \mu ) CMOS</td>
<td>0.18 ( \mu ) CMOS (simulation)</td>
<td>0.18 ( \mu ) 0.18 ( \mu ) CMOS</td>
<td>0.18 ( \mu ) CMOS (simulation)</td>
<td>0.13 ( \mu ) CMOS</td>
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<tr>
<td>( G_m ) value</td>
<td>100 ( \mu )S</td>
<td>100 ( \mu )S</td>
<td>20 ( \mu )S</td>
<td>470 ( \mu )S</td>
<td>26 ( \mu )S</td>
<td>66.8 ( \mu )S</td>
<td>88 ( \mu )S</td>
</tr>
<tr>
<td>Linearity</td>
<td>IM3 at 20 MHz</td>
<td>THD at 100 kHz</td>
<td>THD at 1 MHz</td>
<td>IM3 at 20 MHz</td>
<td>THD at 100 kHz</td>
<td>THD at 1 MHz</td>
<td>THD at 5 MHz</td>
</tr>
<tr>
<td>Input swing range</td>
<td>( 1.3 V_{pp} )</td>
<td>( 2V_{pp} )</td>
<td>( 0.6V_{pp} )</td>
<td>( 0.9V_{pp} )</td>
<td>( 0.7V_{pp} )</td>
<td>( 0.8V_{pp} )</td>
<td>0.4( V_{pp} )</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>3.3 V</td>
<td>2.6 V</td>
<td>1.8 V</td>
<td>1.5 V</td>
<td>1.0 V</td>
<td>1.0 V</td>
<td>1.0 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>10.5 mW</td>
<td>1.7 mW</td>
<td>145 ( \mu )W</td>
<td>9.5 mW</td>
<td>183 ( \mu )W</td>
<td>70 ( \mu )W</td>
<td>45 ( \mu )W</td>
</tr>
<tr>
<td>Figure of merit (FOM)</td>
<td>86</td>
<td>74</td>
<td>82</td>
<td>93</td>
<td>86</td>
<td>90</td>
<td>93</td>
</tr>
<tr>
<td>Input noise spectral density</td>
<td>75nV/( \sqrt{Hz} )</td>
<td>–</td>
<td>–</td>
<td>23nV/( \sqrt{Hz} )</td>
<td>–</td>
<td>–</td>
<td>30nV/( \sqrt{Hz} )</td>
</tr>
</tbody>
</table>
Fig. 13 shows the calculated and simulated $HD_2$ versus the mismatch in the input transistors M3 from 1% to 5%. Fig. 14 shows the simulated $THD$, $HD_5$, and $HD_2$ versus the mismatch in the input transistors M3 from 0% to 5%, the $THD$ is degraded to $-51.3$ dB for 2% mismatch and to $-45$ dB for 5% mismatch. Fig. 15 shows the simulated $THD$, $HD_5$, and $HD_2$ versus the mismatch in the weak inversion transistors M4 from 0% to 5%. It is noticeable that the concept of canceling the 3rd-order harmonic distortion is not affected, and the degradation in the $THD$ is due to the $HD_2$.

The simulation predicts that, for 2% mismatch error in $V_{th}$, the degradation in $THD$ is from $-55.4$ dB to $-54.5$ dB, and for 5% mismatch error, the $THD$ will be $-53$ dB.

### 3. Common-mode feedback (CMFB) circuit

A CMFB circuit is needed for two reasons: (1) to fix the common-mode voltage at high impedance nodes. (2) to suppress the common-mode signal components. Fig. 13 shows the implementation of the CMFB circuit; it must present very small impedance for the common-mode signals but be transparent (very high impedance) for the differential signals. The common-mode open loop impedance $R_{cmfb} = \frac{1}{g_{cmfb}(s)}$ is determined by the small-signal transconductance of the common-mode loop. The parasitic pole of the common-mode loop is associated with the current mirror at node $p$ in Fig. 16 and reduces the loop gain at higher frequency.

$$g_{cmfb} = \frac{g_{cm}}{1 + \frac{C_p}{g_{mp}}}$$

### 4. Implementation and application

Table 1 summarizes this work and compares it with previously reported works. The figure of Merit ($FoM$) defined in (16) is used to compare with different transconductor implementations:

$$FoM = 10\log\left(\frac{G_m \times V_{sw} \times f_0}{p \times THD_{linear}}\right)$$

The $FoM$ takes into account the transconductance value $G_m$, linearity performance $THD_{linear}$, speed of the implemented circuit $f_0$, input swing range $V_{sw}$, and the power consumption $p$, into account.

A 4th-order Butterworth filter has been implemented using the proposed transconductor in 130 nm CMOS technology. The filter architecture is shown in Fig. 17. It operates from 1.0 V single supply. It has eight transconductors of the same value $G_m = 88 \mu A/V$. Note that the transconductors sharing the same output will have one CMFB circuit. The value of $C_1$, $C_2$, $C_3$, and $C_4$ is 3.658 pF, 2.143 pF, 1.515 pF, and 5.173 pF, respectively. The capacitors are implemented using metal-insulator-metal (MIM) capacitors with density 1.5 fF/μm². Fig. 18 shows the 3rd-order intermodulation distortion $IM3$ of the filter to be $-52$ dB for two tones of frequency 2 MHz and 2.1 MHz with differential input of 0.4 $V_{pp}$.

<table>
<thead>
<tr>
<th>MOSFETs</th>
<th>W/L (μm/μm)</th>
<th>Bias current</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1−M3−M8−M9</td>
<td>1/0.35</td>
<td>5 μA</td>
</tr>
<tr>
<td>M2−M10</td>
<td>5.5/0.12</td>
<td>10 μA</td>
</tr>
<tr>
<td>M4</td>
<td>0.4/0.35</td>
<td>8 nA</td>
</tr>
<tr>
<td>M5</td>
<td>1/0.35</td>
<td>0.5 μA</td>
</tr>
<tr>
<td>M6</td>
<td>1/0.2</td>
<td>5 μA</td>
</tr>
<tr>
<td>M7−M11−Mp</td>
<td>4/0.5</td>
<td>5 μA</td>
</tr>
<tr>
<td>M_{cm}</td>
<td>3/0.12</td>
<td>2.5 μA</td>
</tr>
</tbody>
</table>
Fig. 19 shows the layout of the transconductor circuit occupying an area of 0.0011 mm². The layout of the 4th-order Butterworth filter occupies an area of 0.035 mm² and is shown in Fig. 20. Fig. 21 shows the filter’s frequency response before and after the layout.

5. Conclusions

A linear transconductor suitable for low voltage and low power applications is presented. The proposed transconductor was implemented in 130 nm CMOS technology. It operates from 1.0 V supply and achieves a THD of $-55$ dB for differential input signal of $0.4V_{pp}$ after the implementation of the mobility reduction compensation technique. The input referred thermal noise spectral density is $30 \text{nV/ } \sqrt{\text{Hz}}$. A 4th-order 5 MHz Butterworth Gm-C filter has been designed using the proposed transconductor. It achieves a THD of $-53$ dB for $0.4V_{pp}$ differential input. The filter’s active area is 0.035 mm² and it consumes 345 $\mu$W.

References


