A FAST AND LOW SETTLING ERROR CONTINUOUS-TIME COMMON-MODE FEEDBACK CIRCUIT BASED ON DIFFERENTIAL DIFFERENCE AMPLIFIER

TOHID MORADI KHANESHAN†,§, SAEED NAGHAVI‡,¶, MOJDE NEMATZADE†, KHAYROLLAH HADIDI†, ADIB ABRISHAMIFAR‡ and ABDOLLAH KHOEI†

†Microelectronics Research Laboratory, Urmia University, Urmia, Iran
§Microelectronics Research Laboratory, Iran University of Science and Technology, Tehran, Iran
¶t.moradi@urmia.ac.ir
†saeed_naghavi@elec.iust.ac.ir

Received 12 September 2013
Accepted 21 December 2013
Published 10 February 2014

A high-speed and high-accuracy continuous-time common-mode feedback block (CMFB) is presented. To satisfy speed and accuracy requirements, some modifications have been applied on differential difference amplifier (DDA) CMFB circuit. The proposed method is applied to a folded cascode op-amp with power supply of 3.3 V. In order to verify the proposed circuit, simulations are done in 0.35 μm standard CMOS technology. In the worst condition when the output common-mode (CM) voltage is initialized to VCC or GND, only 1.1 ns is required to set the output CM voltage on the desired level. Also in a wide range of input CM voltage variations, the deviation of the output CM voltage from reference voltage is less than 6 mV, so simulation results confirm the expected accuracy and speed while simultaneously the proposed CMFB circuit preserves other characteristics of DDA CMFB circuit such as unity gain frequency, 3-dB bandwidth, phase margin and linearity.

Keywords: Folded; cascode amplifier; common-mode feedback block (CMFB); fully differential op-amp; continuous-time; high-speed; high-accuracy.

1. Introduction

By scaling down of CMOS technology, supply voltages and transistors channel length are shrunk. This improves efficiency of digital circuits; however, in analog
circuits reduction of the voltage headroom will restrict the output swing of the op-amps. Dynamic range of op-amps can be improved by using fully differential structures.  

Fully differential op-amps have many advantages over their single-ended counterparts, such as: (1) larger output voltage swing for a given voltage rail, (2) better immunity to supply and common-mode (CM) noise and (3) lower even-order harmonics. On the other hand, doubling in most parts of the circuit and requiring additional negative feedback control circuit, referred to as the CM feedback circuit, are disadvantages of fully differential structures. Using fully differential op-amps in a feedback application, applied feedback determines differential signal voltages, but does not affect CM output voltage. Therefore, it is necessary to add a common-mode feedback block (CMFB) circuit to stabilize voltage at a proper CM voltage that maximizes the op-amp output swing.

Figure 1 illustrates conceptual architecture of the CMFB. The basic idea in this figure is to sense the level of the output CM voltage, compare it with a reference voltage and feedback the CM correction signal to the amplifier. The correction signal is a function of difference between output CM signal and the reference voltage. There are two approaches to design CMFB circuits. One is the continuous-time and the other is the switched-capacitor. Although switched-capacitor CMFB (SC-CMFB) circuits do not impose any limitation on the output swing of the op-amp and have enough accuracy and low static power consumption, they reduce op-amp’s unity gain frequency and slew rate and also occupy large area. Moreover, SC-CMFBs suffer from clock feed-through and channel charge injection errors and increase op-amp’s load capacitance. Hence, SC-CMFBs are usually used in switched-capacitor applications rather than continuous-time applications. In spite of the lower linearity and output swing of the continuous-time CMFB (CT-CMFB) circuits compared to the SC-CMFBs, do not load op-amp considerably and they are faster and

![Fig. 1. Conceptual architecture of CMFB circuit.](1450065-2)
occupy smaller area. Differential difference amplifiers (DDAs) are common types of CT-CMFB circuits.

Many CMFB circuits have already been proposed in Refs. 6–9. Also, some studies have been done in order to avoid requiring a CMFB circuit in fully differential circuits.4,10,11 In this paper, to achieve higher speed and accuracy, some modifications have been applied on the DDA CMFB circuit.

2. Circuit Design

2.1. Folded cascode amplifier

Operational amplifiers are important building blocks of almost all analog and mixed-mode circuits, such as switched-capacitor filters and data converters.12 Single stage fully differential op-amps are usually used to achieve higher unity gain frequency due to their fewer poles compared to the multiple stage op-amps. In these circuits, all the expected gain must be achieved in single stage. Therefore, it is better to use cascode structure. Telescopic cascode and folded cascode structures are the two possible topologies to achieve higher gain. Telescopic cascode is faster and consumes less power but limits the input CM range and the output swing. In order to alleviate mentioned drawbacks of telescopic cascode op-amps, folded cascode structure can be used.13 Figure 2 shows a folded cascode op-amp. This structure provides better input common-mode range (CMR) and also better output swing. Furthermore, this structure allows choosing proper overdrive voltage to achieve desired unity gain frequency, without impressing the output swing. Also, it is easier to frequency compensate a folded cascode op-amp (the load capacitor operates as compensation capacitor) rather than a two stage op-amp. In this paper, PMOS transistors are used at the input stage of the op-amp due to low noise, body effect elimination by connecting the body to the source terminal in the n-well technology and covering negative rail (or ground) by single supply.

2.2. DDA CMFB circuit

DDA CMFB circuit shown in Fig. 3 is very common CT-CMFB circuit because it provides enough linearity and output swing. Also, it has large trans-conductance and does not imply any resistive load on the main amplifier.14

To illustrate the operation of DDA CMFB circuit, it is assumed that CM voltage and reference voltage are equal and a same differential voltage is applied to the input of the CMFB circuit.15 Furthermore, assuming that the common-mode gain is negligible, the currents of the differential pairs only depend on their differential input voltages. Therefore, the current of $M_{1C}$ will be equal to the current of $M_{4C}$, and similarly the current of $M_{2C}$ will be equal to the current of $M_{5C}$. As long as the voltage $V_{o^+}$ is equal to the negative of $V_{o^-}$, the current passing through the diode-connected $M_{7C}$ is constant. Therefore, the voltage across the diode-connected $M_{7C}$ will not change. This means that the error correction signal produced by CMFB
circuit is equal to zero and output CM voltage of the op-amp does not get affected. Now, assume the output CM voltage is larger than the reference voltage. This voltage decreases the currents in both $M_{2C}$ and $M_{4C}$, which causes less current to be drawn from $M_{7C}$ and as a result the gate voltage of $M_{7C}$ will increase. Therefore, the currents of CMFB_A and CMFB_B are reduced, consequently the CM voltage is brought back to the reference voltage (or almost the reference voltage). To show the nonlinearity of the DDA CMFB circuit, relation between the current of $M_{7C}$ and op-amp’s differential-mode output voltage should be calculated. This relation is given by Eq. (1). In App. A, the procedure for obtaining this equation is explained.

$$I_{D,M_{7C}} \approx I + \sqrt{2KTV_{\text{error}}} \left(1 - \frac{KV_{\text{od}}^2}{16I} - \frac{K^2V_{\text{od}}^4}{512I^2} - \frac{K^3V_{\text{od}}^6}{8192I^3}\right).$$

(1)

It can be seen that the current $I_{D,M_{7C}}$ contains terms that are proportional to the power of even number of the output differential voltage and the odd harmonics are removed. Equation (1) shows that the differential output voltage affects the current $I_{D,M_{7C}}$ which is undesirable since the ideal CMFB circuit would generate a current $I_{D,M_{7C}}$ that is related to $V_{\text{error}}$ but not to $V_{\text{od}}$. Many papers have been published based on the extend linearity of DDA CMFB circuits such as Refs. 1 and 16.
DC CM gain of CMFB loop must be large enough to keep an accurate control of the CM component. It is notable that very large DC CM gain leads to stability problems. Therefore, frequency compensation needs to be considered. If the DC gain is very low then an asymmetrical swing occurs which degrades the dynamic range. Also, the differential gain of the CMFB circuit must be low but in DDA CMFB circuit, the CM gain is not very high due to the diode connected transistor. Hence this circuit is not very accurate and some modifications must be done to enhance the gain. Using the dashed transistors shown in Fig. 3, the gain will increase but they produce delay in the feedback signal’s path. Equation (2) shows the CM gain of DDA CMFB circuit without the dashed transistors. By neglecting $r_{ds}$:

$$A_{v_{CM}} = \frac{1}{g_{m,7C}} \left( \frac{1}{g_{m,1C}} + \frac{1}{g_{m,2C}} + \frac{1}{g_{m,4C}} + \frac{1}{g_{m,5C}} \right).$$

With dashed transistors:

$$A_{v_{CM}} = r_{ds,\text{buffer}} \left( \frac{1}{g_{m,1C}} + \frac{1}{g_{m,2C}} + \frac{1}{g_{m,4C}} + \frac{1}{g_{m,5C}} \right).$$

Fig. 3. Conventional DDA CMFB circuit.
CMFB circuit must be able to respond to the output CM voltage variations rapidly. The speed of the CMFB circuit is directly proportional to the time derivative of $V_{FB}$:

$$\text{speed} \propto \frac{dV_{FB}}{dt} = \frac{I_{D,M_{7C}}}{C_{FB}},$$

(4)

where $C_{FB}$ is the sum of parasitic capacitances which are in the output of the CMFB circuit and create delay for the feedback signal. According to Eq. (4), small value of the capacitance will increase the speed of the CMFB circuit. In the best condition for DDA CMFB circuit (the dashed transistors are not considered), $C_{FB}$ is:

$$C_{FB} = C_{M_{2c}} + C_{M_{4c}} + C_{M_{7c}} + 2C_{OP-AMP},$$

(5)

where $C_{M_{2c}}$ is the parasitic capacitance of $M_{2c}$, $C_{M_{4c}}$ is the parasitic capacitance of $M_{4c}$, $C_{M_{7c}}$ is gate-source or gate-drain capacitance of $M_{7c}$ and $C_{OP-AMP}$ is the parasitic capacitance of each side of op-amp’s output. Nevertheless, $C_{FB}$ is very large in DDA CMFB circuit. Particularly, the diode connected transistor’s capacitance $C_{M_{7c}}$ has a large value and then, the circuit’s response is very slow. Some modifications must be done to decrease $C_{FB}$ and increase CMFB circuit’s speed.

### 2.3. Proposed CMFB Circuit

The main purpose of the proposed CMFB circuit is to increase the speed and accuracy of the conventional DDA CMFB circuit while simultaneously preserving other characteristics of the DDA circuit such as unity gain frequency, 3-dB bandwidth, phase margin and linearity.

Figure 4 shows the proposed DDA CMFB circuit. This circuit has two CMFB circuits named CMFB$_A$ and CMFB$_B$. The first stage is composed of $M_{1A}$–$M_{7A}$ and the second stage is composed of $M_{1B}$–$M_{7B}$. CMFB$_A$ Controls $V_{o+}$ CM voltage and CMFB$_B$ controls $V_{o-}$ CM voltage. The aspect ratio and the bias current of CMFB$_A$ and CMFB$_B$ are half of the conventional DDA CMFB circuit.

In the proposed CMFB circuit, the basic idea is to remove the diode-connected transistor which applies the error correction signal to the folded cascode op-amp. The diode-connected transistor produces a large delay in the feedback signal’s path. Removing this transistor, the speed of CMFB circuit will increase tremendously. Also significant increase in the DC gain is achieved. As a result, we have a high-accuracy CMFB circuit and dashed transistors are no more needed.

Similar to DDA CMFB circuit, the relation between output current of the proposed CMFB circuit and differential output voltage can be calculated. Table 1 shows transistor aspect ratios and Table 2 shows bias voltages of the proposed circuit.

With the same assumptions, the output current can be simplified as follows:

$$I_{\text{CMFB}_A} = I_{\text{CMFB}_B} \approx I - \sqrt{2KI_{\text{error}}} \left( 1 - \frac{KV_{\text{od}}^2}{16I} - \frac{K^2V_{\text{od}}^4}{512I^2} - \frac{K^4V_{\text{od}}^6}{8192I^4} \right).$$

(6)
A Fast and Low Settling Error Continuous-Time CM Feedback Circuit

Fig. 4. Proposed DDA CMFB circuit.

Table 1. Transistor aspect ratios of the proposed circuit.

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Aspect ratio (W/L)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M7, M9, M10, M5A, M5B</td>
<td>90/0.35</td>
</tr>
<tr>
<td>M3, M4</td>
<td>60/0.35</td>
</tr>
<tr>
<td>M5, M6</td>
<td>35/0.35</td>
</tr>
<tr>
<td>M1A, M2A, M3A, M4A, M1B, M2B, M3B, M4B</td>
<td>15/0.35</td>
</tr>
</tbody>
</table>

Table 2. Bias voltages of the proposed circuit.

<table>
<thead>
<tr>
<th>Bias source</th>
<th>Volt</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1</td>
<td>0.8</td>
</tr>
<tr>
<td>B2</td>
<td>1.6</td>
</tr>
<tr>
<td>B3</td>
<td>1.8</td>
</tr>
<tr>
<td>B4</td>
<td>2.2</td>
</tr>
<tr>
<td>REF</td>
<td>1.65</td>
</tr>
</tbody>
</table>
In this circuit such as DDA CMFB circuit, we can use the proposed circuits in Refs. 1 and 17 to extend the linearity of the circuit.

For the DC gain of each side we have:

$$A_{v_{CM,A}} = R_{out,A} \left( \frac{1}{g_{m,1A}} + \frac{1}{g_{m,2A}} + \frac{1}{g_{m,4A}} + \frac{1}{g_{m,5A}} \right),$$

where

$$R_{out,A} = \left( 1 + \frac{g_{m,1A}}{g_{m,2A}} \right) r_{ds,1A} + \left( 1 + \frac{g_{m,5A}}{g_{m,4A}} \right) r_{ds,2A}.$$  

Same equation for the DC gain of $B$ side can be achieved. For the total CM gain we have:

$$A_{v_{CM}} = \frac{A_{v_{CM,A}} + A_{v_{CM,B}}}{2}.$$  

Because the negative feedback is applied to the cascode nodes, the gain of main amplifier and CMFB circuit are equal. Therefore high accuracy and high speed CMFB circuit will be achieved.

In order to evaluate the speed of the proposed circuit according to the definition expressed in DDA CMFB section, first we calculate the capacitance of the output node

$$C_{FB} = C_{M_{1A}} + C_{M_{2A}} + C_{OP-AMP}.$$  

According to Eq. (10), the output capacitance of the proposed circuit is very low and therefore, the speed of this circuit will be high tremendously.

3. Simulation Results

Due to finite CMFB loop gain, output CM voltage is not exactly equal to the desired reference voltage. Therefore, according to Eq. (6), the op-amp differential mode output, affects the current $I_{CMFB_A}$ (similarly $I_{CMFB_B}$) and causes output CM voltage not to be constant. First, to verify the accuracy of Eq. (6), it is simulated in MATLAB and the results are compared with $I_{CMFB}$ which is obtained from SPICE simulation. The simulation parameters are $k = \frac{1}{2} \mu C_{ox} = 105 \mu A/V^2$, $V_{error} = 10 \text{mv}$, $f = 19.72 \text{MHz}$ and $V_{od} = A_d V_m \cos(2\pi ft)$. A fast-fourier transformation (FFT) is performed on the CM sense currents, $I_{CMFB_A}$ and $I_{CMFB_B}$, obtained from both SPICE and MATLAB simulations, and the FFT spectrums are shown in Fig. 5.

As it can be seen in Fig. 5, the SPICE simulation result shows a good matching to the MATLAB result. The difference between grass level of the SPICE and MATLAB
(results is due to that the MATLAB simulation uses Eq. (6) which has an ideal behavior but in SPICE simulation other non-idealities can affect the $I_{CMFB}$ linearity.

In order to evaluate the performance of the proposed DDA CMFB circuit, it is realized in a folded cascode fully differential op-amp. Figure 6 shows the transient response of the proposed CMFB circuit with initial condition equal to 0 and VCC. It is apparent that within less than 1.1 ns, the output CM voltage settles to 95% of the final value. This result shows that the proposed CMFB circuit can control the output CM voltage with the voltage variations very quickly. The characteristic of the output CM voltage error versus the input CM voltage variation is important to evaluate the

![Graph](image)

**Fig. 6.** Transient response of the output CM voltage.
accuracy of CMFB. This is shown in Fig. 7. As the simulation result shows, the maximum deviation of the output CM voltage is found to be very small, e.g., about 0.5 mV for 1.65 V of the input CM voltage. Therefore, the proposed CMFB circuit has a high accuracy and in a wide range of the input CM voltage variation can fix the output CM voltage in the desired level.

Comparison of frequency response of the proposed circuit with frequency response of the conventional DDA CMFB circuit shows that the bandwidth of the proposed circuit is the same as the conventional one. Therefore bandwidth of the system depends on topology of the op-amp and the proposed circuit has no negative impact on it.

![Fig. 7. Output CM voltage error: (a) 1 < \( V_{IN,CM} < 2.2 \) and (b) 0 < \( V_{IN,CM} < 3.3 \).](image)

![Fig. 8. Output spectrum of op-amp.](image)
The output differential-mode voltage spectrum of the op-amp is shown in Fig. 8. Applying a 19.72 MHz sinusoidal input with the amplitude of 2 mV results in an output THD less than $\frac{58}{\text{dB}}$ (input level $\frac{71}{\text{dB}}$).

Figure 9 shows transient response of the output CM voltage for 10% variation of bias voltages, 2% variation of transistors threshold voltage and temperature variation from $\frac{55}{\text{C}}$ to $\frac{125}{\text{C}}$.

Also Fig. 10 shows the transient response of the output CM voltage for the proposed circuit by applying the above-mentioned three kinds of the variances simultaneously. As it can be seen, the transient response of the proposed circuit in this condition confirms the expected accuracy and speed.

Layout of the proposed circuit is depicted in Fig. 11(a) and post layout simulation is shown in Fig. 11(b). Simulation results verify that despite these possible variations, proposed circuit provides expected performance. Also post layout simulation shows that the proposed circuit can work correctly and efficiently. Also, power
The consumption of the proposed CMFB circuit is the same as the conventional DDA CMFB circuit and this circuit does not impose power overhead.

Table 3 summarizes the performance of the proposed CMFB circuit and compares it to the several reported works. It can be observed that the proposed architecture is very fast and also it can achieve a high accuracy.

![Fig. 10. Transient response of the output CM voltage for all three kinds of variances.](image)

![Fig. 11. (a) Layout of the proposed circuit and (b) post layout simulation.](image)

Table 3. Performance summary and comparison.

<table>
<thead>
<tr>
<th></th>
<th>This work</th>
<th>Ref. 5</th>
<th>Ref. 7</th>
<th>Ref. 18</th>
<th>Ref. 19</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (μm)</td>
<td>0.35</td>
<td>0.18</td>
<td>2</td>
<td>0.18</td>
<td>0.35</td>
</tr>
<tr>
<td>Supply voltage (V)</td>
<td>3.3</td>
<td>1.8</td>
<td>5</td>
<td>0.9</td>
<td>3.3</td>
</tr>
<tr>
<td>Settling speed</td>
<td>1.1 ns</td>
<td>4 ns</td>
<td>2 μs</td>
<td>30 ns</td>
<td>12 ns</td>
</tr>
<tr>
<td>Settling error (mV)</td>
<td>0.35</td>
<td>—</td>
<td>0.4</td>
<td>≈1</td>
<td>36</td>
</tr>
</tbody>
</table>
4. Conclusion

A continuous-time differential difference CM feedback circuit is presented. The proposed CM feedback block is applied to a 3.3 V folded cascode amplifier and the amplifier with embedded CMFB circuit is simulated in 0.35 μm standard CMOS technology. To evaluate the speed of CMFB circuit, the transient response of the output CM voltage is studied. With the initial condition equal to zero and VCC to the output CM voltage, only 1.1 ns is required to set the output CM voltage on the desired level. Moreover, characteristic of the output voltage error shows that in the range of 1 V to 2.2 V for the output CM voltage, its error is not more than 6 mV in the worst condition. Therefore, the simulation results confirm the expected accuracy and speed.

Simulation results verify that despite bias voltage, threshold voltage and temperature variations proposed circuit provides expected performance. Also post layout simulation shows that the proposed circuit can work correctly and efficiently.

Also, the other characteristics of the proposed CMFB circuit such as the unity gain frequency, DC gain, phase margin, power consumption, are the same as the conventional DDA CMFB circuit and proposed CMFB circuit has no negative impact on them.

Appendix A. Nonlinearity of the DDA CMFB Circuit

To show the nonlinearity of the DDA CMFB circuit, relation between the current of \( M_{7C} \) and op-amp’s differential-mode output voltage should be calculated. For simplification, it is assumed that all transistors are in the saturation region. Neglecting the second order effects, the drain current of the MOS transistor is given by the following expression:

\[
I_d = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_T)^2, \tag{A.1}
\]

where \( \mu_n \) is the effective carrier mobility, \( W \) is the gate width, \( L \) is the gate length, \( C_{ox} \) is the gate oxide capacitance per unit area and \( V_T \) is the threshold voltage of the MOS transistor. Considering the nonlinearity analysis derived from Refs. 1 and 16 and assuming that the differential pairs and current sources are matched due to the similarity of \( M_{1C}, M_{2C}, M_{4C} \) and \( M_{5C}, \frac{1}{2} \mu_n C_{ox} \) are equal between these transistors and is taken to calculation as \( K \). Applying Kirchhoff’s voltage law around source loop of \( M_{1C} - M_{2C} \), we have:

\[
V_{o^+} - V_{gs,M_{1C}} + V_{gs,M_{2C}} - V_{REF} = 0. \tag{A.2}
\]

Also considering the currents at node \( p \), we have:

\[
I_{D,M_{1C}} + I_{D,M_{2C}} = I_{D,M_{3C}} = I. \tag{A.3}
\]
Combining (A.1)–(A.3) results:

\[ I_{D,M_C} = \frac{I}{2} + \sqrt{\frac{I \cdot K}{2}} (V_o^+ - V_{REF}) \sqrt{1 - \frac{K \cdot (V_o^+ - V_{REF})^2}{2I}}. \]  

(A.4)

Similarly for the current \( I_{D,M_{4C}} \), we can write:

\[ I_{D,M_{4C}} = \frac{I}{2} + \sqrt{\frac{I \cdot K}{2}} (V_o^- - V_{REF}) \sqrt{1 - \frac{K \cdot (V_o^- - V_{REF})^2}{2I}}. \]  

(A.5)

The drain currents of \( I_{D,M_C} \) and \( I_{D,M_{4C}} \) form \( I_{D,M_{7C}} \)'s current. Then:

\[ I_{D,M_C} + I_{D,M_{4C}} = I_{D,M_{7C}}. \]  

(A.6)

As a result, using (A.4)–(A.6) for \( I_{D,M_{7C}} \)'s current, we have:

\[
I_{D,M_{7C}} = I + \sqrt{\frac{I \cdot K}{2}} \left[ (V_o^+ - V_{REF}) \sqrt{1 - \frac{K \cdot (V_o^+ - V_{REF})^2}{2I}} + (V_o^- - V_{REF}) \sqrt{1 - \frac{K \cdot (V_o^- - V_{REF})^2}{2I}} \right].
\]

(A.7)

Equation (A.7) can be simplified as:

\[
I_{D,M_{7C}} = I + \sqrt{\frac{I \cdot K}{2}} \left[ \frac{K \left( V_{error} + \frac{V_{od}}{2} \right)^2}{2I} \left( V_{error} + \frac{V_{od}}{2} \right) + \left( V_{error} - \frac{V_{od}}{2} \right) \sqrt{1 - \frac{K \left( V_{error} - \frac{V_{od}}{2} \right)^2}{2I}} \right],
\]

(A.8)

where \( V_{error} = V_{CM} - V_{REF} \) is the deviation of the op-amp output CM voltage from the desired CM reference voltage and \( V_{od} = V_o^+ - V_o^- \) is the output differential-mode voltage of the op-amp.

Assuming, \(|V_{error}| \ll |V_{od}| \) Eq. (A.8) becomes:

\[ I_{D,M_{7C}} \approx I + \sqrt{2KI} V_{error} \sqrt{1 - \frac{K V_{od}^2}{8I}}. \]  

(A.9)

Substituting Taylor series for the square root terms of Eq. (A.9) and keeping the first four terms in the series yields:

\[ I_{D,M_{7C}} \approx I + \sqrt{2KI} V_{error} \left( 1 - \frac{K V_{od}^2}{16I} - \frac{K^2 V_{od}^4}{512I^2} - \frac{K^3 V_{od}^6}{8192I^3} \right). \]  

(A.10)
References


2. E. S. Sinencio, Common-mode control techniques for low voltage continuous-time analog signal processors, Texas AM University lectures (2000).


