Low-Power Linear-Phase Delay Filters for Neural Signal Processing: Comparison and Synthesis

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Abstract—We present the design and implementation of linear-phase delay filters for ultra-low power neural signal processing. The filters are intended to implement a low-distortion delay element for automatic biopotential detection in neural recording implants. Continuous-time OTA-C filters are used to realize a 9th-order equiripple transfer function presenting a constant group delay. This analog delay allows to process neural waveforms with reduced overhead compared with digital delays. An allpass transfer function is used to implement such analog delay because it achieves wider constant-delay bandwidth than all-pole does. Two filters realizations are compared for implementing it: the Cascaded structure and the Inverse follow-the-leader feedback filter. Their respective strengths and drawbacks are assessed by modeling parasitics and non-idealities of OTAs, and using transistor-level simulations. A power budget of 200 nA is used in both filters. Experimental measurements with the chosen topology are presented and discussed.

Index Terms—Neural signal processing, Neuroprosthetics, Linear-phase delay filter, Cascaded filter, Inverse Follow-the-Leader Feedback, Ultra-low power OTA-C filters.

I. INTRODUCTION

Recording extracellular neural biopotentials from several neurons in the cortex has become a necessity for research in neuroscience. This experimental approach promises the development of new prosthetics to treat various neural disorders including motor impairments, epilepsy, and paralysis. The main mechanism of information transmission in extracellular neural recording waveforms is a change in action potential (AP) generation rate by individual neurons. There is a great interest in automatic detectors for use in neural prosthetics. A suitable detector must locate AP occurrences and capture as much waveshape features as possible (time of occurrence, general shape, etc.) for further processing such as waveform sorting. Additionally, detectors must drain very low power for use in dense devices presenting high-channel counts. An automatic detection strategy was presented in [1] to preserve complete waveforms integrity by means of a delay element implemented with an ultra-low power continuous-time filter. Such filter introduces a linear-phase shift over the bandwidth of interest with very low distortion to achieve the required delay. However, implementing a suitable neural signal delay requires a high-order filter which presents higher sensitivity to parasitics and circuits non-idealities. Moreover, achieving ultra-low power in CMOS circuits requires operating MOS devices in the weak inversion regime which exhibit poor matching and higher sensitivity to process variation. Therefore, particular attentions must be paid to minimize these effects in the design of such delay filter.

This paper proposes a comparative study of two ultra-low power continuous-time filter structures suited to implement the required delay element. Effects of parasitics and non-idealities are assessed employing analytical and Verilog modeling approaches, and transistor-level simulations. We first highlight advantages and drawbacks of each topology, and then present the experimental results obtained with fabricated test chips.

II. CONSTANT DELAY FILTER DESIGN

APs are weak amplitude signals (50–500 µV) in the 100 Hz −10 kHz frequency band whose duration is of a few milliseconds. The rate of occurrence of APs varies from 10 to 120 per second [2]. In the detector presented in [1], a delay is induced to provides delayed copies of APs and shift the waveform back to its onset right upon detection. A time delay of about 600 µs is needed, which gives approximately a third of a typical AP duration.

A. Transfer Function Requirements

A constant group delay is required in the filters to achieve low-distortion within the neural signal bandwidth. The equiripple delay filter can achieve a wider constant-delay bandwidth (noted \( \omega_{CD} \)) than other filter responses because it distributes the permitted delay error uniformly over the passband [3]. However, this response doesn’t have any close form transfer function, and its coefficients must be obtained numerically. The \( \omega_{CD} \) of an equiripple response is approximated by

\[
\omega_{CD} = \frac{\omega_c \omega_e}{2\pi},
\]

where \( \omega_c \) is a normalising frequency, and \( \omega_e \) is the normalized constant-delay bandwidth. We have that \( \omega_c \) is the inverse of the desired delay \( D \) multiplied by a constant \( D_0 \) that is \( \omega_c = D_0 \times (1 / D) \), where \( D_0 \) is the intrinsic delay of the equiripple filter. Constants \( D_0 \) and \( \omega_e \) are function of the filter order. Moreover, the filter uses an allpass transfer function because the presence of transmission zeros makes its delay twice as that of an all-pole filter of equal degree, which is such that \( D_{AP} = 2D \). The tabulated values for a 9th-order equiripple filter with 5% delay error are \( \omega_e = 3.66 \) and \( D_o = 2.93 \). Using \( D = 300 \) µs...
(i.e., $D_{10} = 600 \mu s$) to calculate $\omega_c$ and replacing these values in (1) gives a $\omega_{CD}$ of 5.7 kHz, which is well suited for this application because this band contains most neural signal energy. Allpass filters exhibit magnitudes equal to unity for all frequencies. This imposes the numerator $N(s)$ and the denominator $D(s)$ in the transfer function to be complex conjugates. Thus, the required ninth-order filter has the form

$$H(s) = \frac{D(-s)}{D(s)} = \frac{-b_N s^N + b_{N-1} s^{N-1} + \ldots + b_1 s + b_0}{b_N s^N + b_{N-1} s^{N-1} + \ldots + b_1 s + b_0}.$$  

(2)

Fig. 1 shows the ideal phase response and group delay of the 9th-order equiripple filter whose coefficients were taken from [4].

B. OTA-C Delay Filter Synthesis

Synthesizing high-order filters requires particular attentions to minimize circuit non-idealities and parasitics because they present more sensitivity than lower-orders. The selected filter topology must use a small amount of components and mitigates non-ideal effects. OTA-C filter topologies have shown excellent performances in low-power systems because they allow for high-order filter implementations with the least number of active devices and passive components counts. Several examples of such low-power high-order OTA-C filters have been implemented and used in medical applications [5-8]. Low-power, small-gm OTAs and small-size integrated capacitors are employed to implement the delay filters.

A manifold of topologies has been proposed and tested to decrease the components count and provide better versatile transfer functions. Notably, an inverse-follow-the-leader feedback topology (IFLF) [4, 9] has a compact form and allows to synthesize general nth-order transfer functions with poles and arbitrary finite transmission zeros. Besides, the Cascaded filter topology is known for its simplicity of implementation. Both topologies are compared for the implementation of the required equiripple transfer function. The filters use grounded capacitors and single-ended OTAs to minimize the parasitic poles (which cause excess phase shift) and avoid the generation of parasitic zeros. Grounded capacitors absorb parasitic capacitances and need smaller area than floating ones [9]. Also, small-area nMOS and pMOS devices are used in the OTAs to minimize input and output parasitic capacitances. Moreover, cascode transistors increase the impedance of the output stage. A unique capacitor value of $C = 1 \text{pF}$ is used within both structures for simplicity. Fig. 2 presents both OTA-C filter topologies implementing the transfer function in (2). Their coefficients are implemented by $g_m$ ratios of OTAs, whereas $\omega_{CD}$ scales with capacitor values.

The schematic of IFLF filter, which uses an input distribution network [3], is presented in Fig. 2a. The general expression for the complete transfer function can be found in [3]. The allpass transfer function requires $g_m = 2g_i$, when $i$ is odd, otherwise $g_m = 0$. The Cascaded filter (Fig. 2b) uses one first-order allpass section cascaded with four subsequent biquadratic allpass sections presenting growing quality factor for improving the overall linearity. The biquadratic sections are synthesized according to an allpass equal-capacitor-values topology, introduced in [10], which yields a minimum number of components. Each biquad uses four OTAs and two equal-value capacitors to implement the required polynomial. We must have $g_m = g_9$ in each stage for the transfer function to have a unity gain. The 9th-order IFLF and Cascaded filters use 17 and 18 OTAs respectively, and nine 1-pF capacitors each.

III. OTAs NON-IDEALITIES AND PARASITIC EFFECTS

The input and output capacitances, noted $C_{in}$, $C_{out}$, respectively, and the finite output resistance $R_{out}$ are taken into account for both filters. The parasitics are added in the ideal filters and the modified transfer functions including parasitics are derived. These updated transfer functions were used to adjust each $g_m$ in order to correct the unwanted effects. Then the model is further extended by taking into account the dependency of $g_m$ over the frequency in each OTA with a single pole model for $g_m(f)$. The resulting models for the 9th-order transfer function with frequency dependency were not derived analytically because of their overwhelming complexities. Instead, they were described with Verilog-A building blocks and simulated with Spectre. The simulated filter models show that having too small 3-dB frequencies ($f_{3db}$) in the OTAs can cause error in the magnitude of the frequency responses and change the shape of the delays. The $f_{3db}$ in the OTA scales with $g_m$ and the bias current. The model shows that $f_{3db}$ in general are lower for the IFLF than for the
Cascaded filter. Overall, $C_{in}$ appears to be the parameter that has the most influence on the transfer functions. Parameters $C_{out}$ are absorbed by the filter capacitors $C$ which exhibit bigger values. The Cascaded filter has been found less sensitive to the effects of the frequency dependent $g_m(f)$. Also, the IFLF group delay presents a large peak near $\omega_{CD}$ whereas the group delay of the Cascaded filter remains pretty flat. This higher sensitivity is most likely due to its multiple feedback structure.

IV. CIRCUIT IMPLEMENTATIONS

OTAs whose transistors are biased in the weak inversion regime are used in both filter topologies. Subthreshold operation of MOS devices allows circuits to achieve ultra-low power consumption and to operate in the very-low portion of the frequency spectrum (0 to 10 kHz), where lie most bioelectrical signals. A total supply current of 200 nA is used in both filter topologies.

A. Subthreshold OTA

Currents on the order of one nA to a few tens of nA are used in the OTAs to address power and $g_m$ sizes. However, operation at very low current comes at the cost of a reduced dynamic range ($DR$). Therefore, the chosen OTA circuit incorporates source degeneration ($M_{S1}$, $M_{S2}$) and bump linearization ($M_{B1}$, $M_{B2}$) in the diff-pair to simultaneously achieve low overall $g_m$ and a better linear range. The subthreshold $g_m$ are individually adjusted by scaling the bias currents in the diff-pair of each OTA. The bias current used in the OTAs range from 0.6 nA to 21 nA for the IFLF, and from 1.5 nA to 30 nA for the Cascaded filter, so the required $g_m$ can be implemented within the prescribed power budget.

B. Mismatch and Process Variations

A problem with MOS transistors operating in weak inversion is the poor matching between devices. Mismatch causes random changes in the drain current of MOSFETs, and thus in their $g_m$. In this design, mismatch affects the overall $g_m$ of OTAs and generates input-referred offset that can saturates some OTAs and render the filters unfunctional. Mismatch and process variation can be reduced by means of adequate layout techniques such as interdigilated structures, and common-centroid configurations. Careful matching of MOS diff-pairs and current mirrors has shown to enables for good performances in subthreshold filters [11]. Matching is greatly improved by distributing currents instead of voltages, and by local mirroring of currents [7]. Moreover, a tuning strategy is recommended in [8] to reduce mismatch and process variation effects.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Transistor-Level Simulation

The linear-phase delay filter is compared with its digital counterpart, a 16-depth, 8-bits FIFO, implementing a 600-μs signal delay, at a sampling rate of 30 kHz (Fig. 5). The analog filter dissipates around 3 times less power than the FIFO. The IFLF and the Cascaded filters performances are compared using transistor-level simulations and Monte Carlo trials. Table I highlights both filters performances. The IFLF clearly presents insufficient dynamic range because it features too much input noise and distortion. Its THD is of 9.6% compared to 1.1% for the Cascaded filter for a same input range of 40 mVpp. The IFLF also shows a high gain sensibility of 20% compared to 6% for the cascade. A figure of merit (FOM) has been defined to assess and compare the performances of low-power filters. It is expressed as

$$FOM = \frac{\text{Power} \cdot V_{DD}^2}{n \cdot f \cdot DR},$$

where $DR$ is the dynamic range, $n$ is the number of poles plus zeros, and $f$, the center frequency for which the result is...
idealities, the Cascaded filter achieves better reported. In addition to exhibit lower sensibility to circuit non-

range of power consumption. This is because the IFLF requires a larger average in the OTAs for the Cascaded filter.

Therefore, higher currents can be used in average in the OTAs for the Cascaded filter.

B. Measured Results

The Cascaded filter has been implemented in a CMOS 0.18-μm six-metal one-poly process and tested with synthetic neural waveforms. Fig. 6 shows a microphotograph of the integrated Cascaded filter. A synthetic neural signal presenting a realistic firing rate was constructed and played at the filter input. Fig. 7 presents the input signal and the delayed filter response. The signal delay was adjusted close to 600 μs by tuning a single external bias current source from which every OTAs bias currents in the design are derived, as suggested in [8]. The measured performances of the filter for ten chips are reported in Table I. Table II compares the fabricated filter with other low-power filter implementations in terms of power per poles plus zeros, and FOM. The FOM achieved is $3.5 \times 10^{-13}$, which is among best reported results.

VI. CONCLUSION

Two OTA-C filter topologies have been compared with respect to effects of parasitics and $g_m$ frequency dependency. The IFLF structure exhibits more sensibility and smaller $DR$ than the Cascaded filter for a same low-power budget. Therefore, the Cascaded filter has been fabricated and tested for integration in a biopotential detector.

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REFERENCES


