Journal of ELECTRICAL ENGINEERING, VOL. 54, NO. 5-6, 2003, 123–127

HIGH SPEED LOW POWER MULTI–THRESHOLD VOLTAGE FLIP FLOPS

Abdoul Rjoub - Ali Shatnawi *

Low-Power High-Speed Flip Flops (LPHSFF) are proposed in this paper. They are based on CMOS multi-threshold voltage techniques. High threshold voltage MOSFET transistors are applied on the non-critical paths of flip-flops in order to suppress the stand-by leakage-current, while low threshold voltage MOSFET transistors are applied on the cross-coupled critical path which in fact is the speed bottle neck of the flip-flip. This happened in order to increase the speed of operation of the circuit and to reduce the power dissipation. The proposed technique is usable in all types of flip-flops. Simulation results show the validity of the proposed technique to save power dissipation and to increase the speed of operation of the circuits. Using SPICE parameters of 0.25 um multi-threshold voltage CMOS technology, simulation results for 2.1 V supply voltage shown that 30% of power dissipation is reduced as the speed of operation is increased by 55%. Different applications are used to demonstrate the validity of the proposed technique.

K e y w o r d s: cross-coupled, critical path, multithreshold technique, leakage-current, low power design, high speed operation, memory cells, flip-flops, feedback output

1 INTRODUCTION

High-speed operations with low power dissipation is becoming a critical factor in the modern design of several electronic components, especially in portable and hand-held devices [1]. Examples of these devices include mobile telephones, hearing-aid devices and palmtops, which are novel multimedia gadgets that require higher signal or data processing capability with low power requirements [2]. In order to achieve these design requirements which are vital for all future high-speed devices, excessive research on low-power technologies supporting high-speed operations is needed [3].

Different types of low power implementations for high speed operation applications are proposed [4][5]. One of the most important techniques to reduce the power dissipation in CMOS circuits is to reduce the supply voltage [6]. In CMOS technology circuits, the power dissipation is approximately proportional to the square of the supply voltage. To achieve the design goals of future devices based on the CMOS technology, it might be inevitable to use a supply voltage less than 1 volt. However, reducing the supply voltage to 1 V could prove to be rather impotent since it results in a drastic degradation in the speed of operation [6]. Hence, in order to support high speed operations using low supply voltage, reduction in the threshold voltage of transistors could be proposed as a solution to this problem [7]. Reducing the threshold voltage by itself is not the absolute optimal solution, as the leakage current of the MOS transistors will be increased [7]. The increase in leakage-current is negligible when compared with the drastic reduction in power dissipation, in applications using low threshold voltage transistors, which is the main theme of this paper.

In order to achieve high-speed operation and low power dissipation at the same time, different techniques can be used. The multi-threshold voltage technique, which combines the use of high threshold voltage transistors and low threshold voltage transistors on a single chip, could be used to achieve this target [8]. The high threshold voltage transistors are used in order to cut-off the leakage-current, while the low threshold voltage transistors are used to reduce the delay time and increase the operation speed of the circuits [9].

Memory cells and registers are built basically from flip-flop circuits [10]. Different types of flip-flops are used and implemented for this purpose [11]. The Set/Reset (SR) flip flop, Jump and Kill (JK) flip-flop, which can overcome the drawback of the Set/Reset flip have been reported in the literature [12]. The D and T flip-flops have also been reported in published research as memory cells[1]. All of these flip-flops are similar in their operation, and are used in many ways as buffers to store or transfer data.

The main drawback of these flip-flops are the relatively high portion of the total chip power consumption, it consumes about 30% from the total power dissipation in MPU2 circuits [11], and the relatively high delay time of their outputs[10][11]. The delay time of a flip-flop is caused from the underlying cross-coupled feedback effects. Because of the feedback, the operation speed is reduced and an increase in the power dissipation is incurred. So it is systematic to design memory cells or register circuits achieving high-speed operation while keeping power dissipation to a minimum level [13] [14].

In this paper, we describe a new implementation for reducing the power dissipation and increasing the operation speed of the flip-flop. In order to achieve this goal, multi-

* Department of Computer Engineering, Jordan University of Science and Technology PO Box 3030 Irbid, Jordan
E-mail: abdoul@just.edu.jo

ISSN 1335-3632

threshold voltage transistors are used: the low threshold voltage transistors are used in the cross coupled latch (which in fact is the critical path of the circuit) in order to increase the operation speed of the flip flop, while the other transistors are maintained at the high threshold voltage in order to cut-off the leakage current. SPICE simulations results verify the validity of the proposed technique. They show that by using this type of design no glitch phenomena occurred, and an increase in operation speed and reduction in the power dissipation are also shown.

In Section II several techniques for low power/high speed operations are introduced. The proposed technique is introduced in Section III. Simulation results, as comparison results between the proposed design and the conventional design are given in Section IV.

2 ISSUES FOR LOW POWER DISSIPATION

In CMOS technology the power dissipation could be summarized in three main issues: dynamic power, short circuit power and leakage power dissipation. The first issue is the dominant power dissipation in modern integrated circuits, it results from charging and discharging the gate capacitances when the input changes from low level voltage to high level voltage. It could be expressed as:

$$P_{\text{dynamic}} = C_{Load} V_{DD}^2 f_{\text{clk}}, \tag{1}$$

were C_{Load} is the total load capacitances, V_{DD} is the supply voltage, and f_{clk} is the operation frequency. As shown from this equation, decreasing the load capacitance could be achieved by reducing the total silicon area as using material with low capacitances in their nature. The power supply voltage (V_{DD}) is the most efficient way to reduce power dissipation, Figure 1 shows the relation between power dissipation and supply voltage. Simulation results in Fig. 1 are given for load capacitor 100 pF, and clock frequency of 1 MHz. Actually, reducing the supply voltage from 3.3 V to 1 V could decrease the power dissipation to one tenth (1/10). A decrease in f_{clk} could be verified if we used parallel or pipelining implementations at a high level architecture [15].

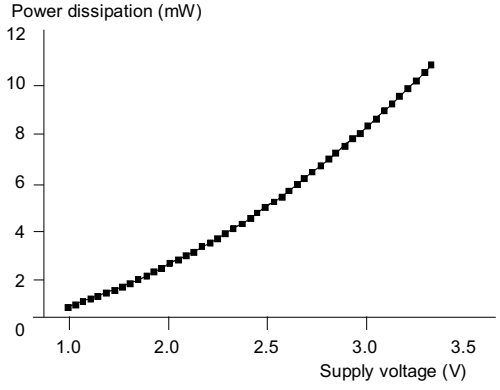

Fig. 1. Relation between power dissipation and the supply voltage

Decreasing the supply voltage in the opposite causes an increased in delay time, so in order to keep the circuit in high speed operation using low supply voltage, we should keep down the threshold voltage of transistors. In general, the gate delay time in CMOS circuits is given by the following equation [6].

$$t_d = \frac{C_L V_{DD}}{I_{ds}} = \frac{C_L V_{DD}}{k(V_{DD} - V_{TH})^2} \tag{2}$$

Here I_{ds} is the drain current in the saturation region, V_{TH} is the threshold voltage of the transistor, and k is a constant depending on the SPICE parameters. It is clearly manifested that lowering the supply voltage decreases I_{ds}, as it inversely proportional to the square of the voltage difference $(V_{DD} - V_{TH})$. The decrease in I_{ds} causes an increase in the gate delay time as V_{DD} approaches V_{TH}. Figure 2 shows the relation between the threshold voltage and the delay time for two values of supply voltages. It seemed very clear that decreasing the supply voltage, the speed operation becomes very sensitive to the threshold voltage of transistor. So it becomes very important to reduce the threshold voltage of the transistor to increase the speed operation of the circuit.

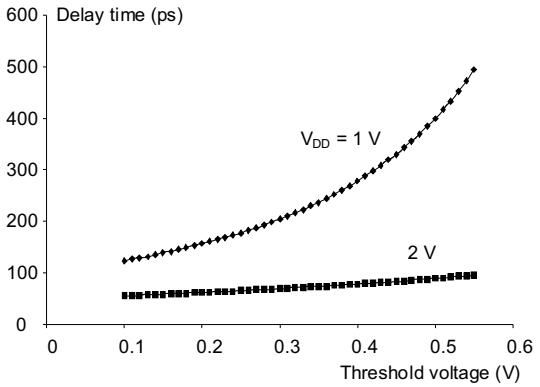

Fig. 2. Delay time dependence on the threshold voltage

Decreasing the threshold voltage is the key factor to reduce the power dissipation. However, keeping the threshold voltage at a minimal value causes an increase in the value of the leakage current, and the value of the leakage current becomes dominating in low power applications. In general, the leakage currents vary exponentially with the threshold voltage as shown in the following equation:

$$I_{\text{leakage}} = \frac{w}{w_0} I_0 \, e^{\frac{V_{GS} - V_{TH}}{n V_{TH}}}, \tag{3}$$

where w is the width of transistor, n is a constant, V_{GS} is the source-gate voltage, and V_{TH} is the threshold voltage of transistor. So as a result to keep down the threshold voltage and reducing the supply voltage Multithreshold voltage technique could be the solution of this problem as declared from the introduction.

3 LOW POWER FLIP FLOP CIRCUITS

The flip-flop is the main component of a memory cell and a register circuit. It is typically used for digital data storage and data transfer from/to different components of a digital system. Several types of flip-flops are used; the most common one is the Set/Reset flip-flop. As an example of the proposed technique, in Figure 3 we show one cell memory based on the Set/Reset flip-flop. Here the shown rectangle depicts a Set/Reset flip-flop based on NAND gates [16], it is triggered to a high state at Q by the set signal (S) and holds that value until reset to low by a high signal at the Reset input (R).

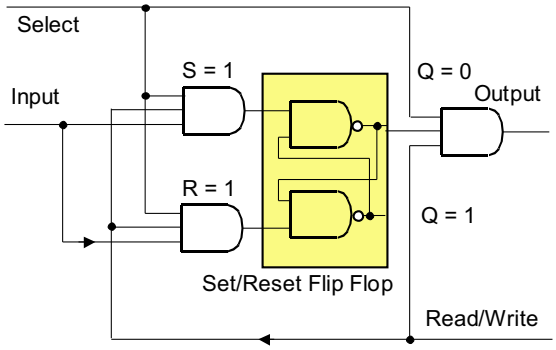

Fig. 3. Basic RAM cell memory using S/R flip-flop [17]

The operation of the flip-flop shown in Fig. 3 is as follows: suppose that the two independent inputs S, R are set to high, if Q is set to low state, then the output of down gate will set to the high state. In this case, the output of up NAND gate should wait a period of time until the output of down gate is produced (yielded); it is the same for down NAND gate and so on for the next stage of flip flops. The delay time at the output of each gate depends on the two cross coupled signals of the NAND gates, in particular, it depends on the threshold voltage of the connected transistors in this critical path configuration. Consequently, it is obvious that the main drawback of this circuit is the cross coupled path, which is the main reason for the increase in the delay time.

This problem can be solved by replacing the cross-coupled transistors by low threshold voltage transistors, which results in an increase in the speed of operation of the feedback, and at the same time reduce the power dissipation as implied by (2). Figure 4 shows the transistor level implementation of the SR flip-flop depicted in Fig. 3. The solution to the problem can by carried out by replacing the transistors of the cross-coupled by low threshold voltage transistors (bold transistors in the figure) with 0.2 V for the n-MOS transistor and -0.25 V for the p-MOS transistor. These threshold values are low enough taken into consideration the low supply voltage of 2.1 V. The other transistors of the circuit that have no relation to the critical path are maintained at the high threshold voltage of 0.5 V for n-MOS transistors and 0.6 V for p-MOS transistors.

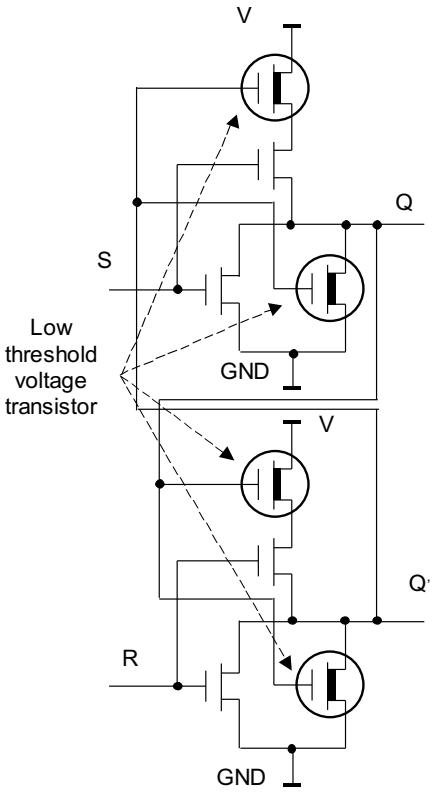

Fig. 4. Multi-threshold voltage Set/Reset flip flop circuit

4 SIMULATION RESULTS

The performance of the proposed technique has been evaluated using SPICE circuit simulator. A 0.25 μm technology with multi-threshold voltage SPICE parameters is used. Different types of flip-flops are designed using the conventional and the proposed design, for comparison purposes. Figure 5 depicts the output waveforms of the D flip flop at port Q, where Q_{mult} is the output using low threshold voltage, while the Q_{Conv} is the output using the conventional design. It clearly shows that the proposed technique is faster than the conventional design both in the rise time and fall time.

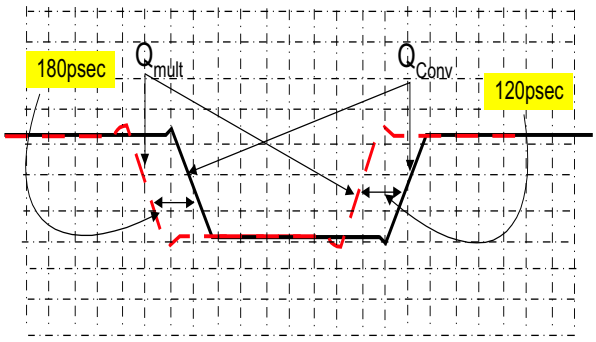

Fig. 5. Output waveform of the D flip-flop

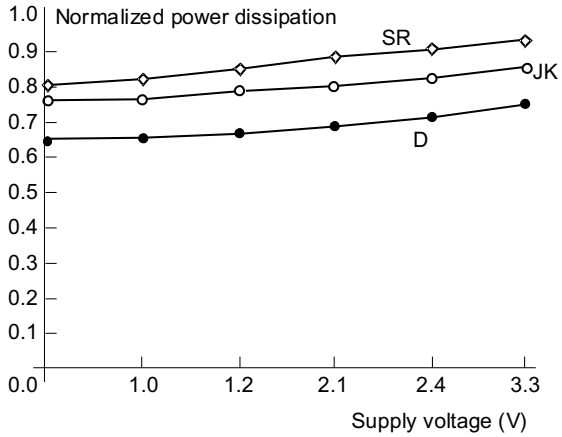

Fig. 6. Normalized power dissipation as a function of power supply voltage

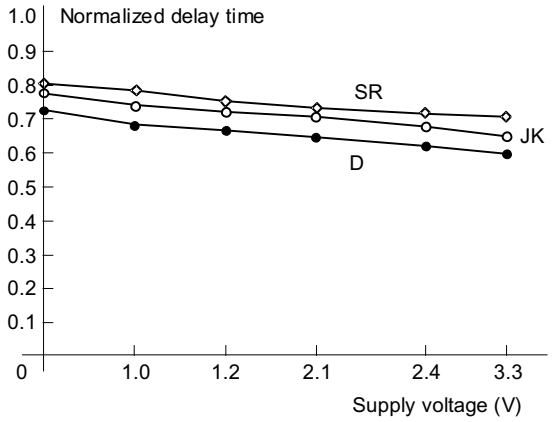

Fig. 7. Normalized delay time as a function of power supply voltage

Figure 6 shows the normalized power dissipation of the conventional and the proposed designs using the same input signals and transistor widths for different values of supply voltage. It shows clearly the improvement of the proposed technique in power dissipation savings for all supply voltages. For the measurements of the power dissipation, the power-meter circuit in [18] is used.

Figure 7 shows also the normalized delay time of the proposed technique as compared with the conventional design for different values of supply voltage. This figure confirms the validly of the proposed technique for high speed operation applications.

Figure 8 shows the normalized energy of the proposed technique in comparison with the conventional design.

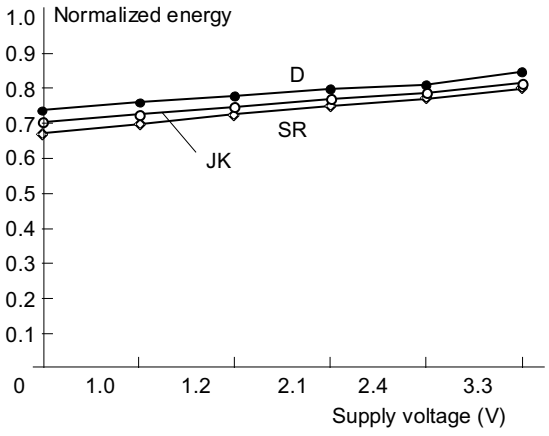

Fig. 8. Normalized energy as a function of power supply voltage

The proposed technique is applied for different applications using three types of flip-flops. Table 1 clearly shows the power dissipation of the proposed technique as compared with the conventional design under the same conditions of transistor width and supply voltage.

Table 1. Normalized power dissipation, in %

FF-type	S/R	J/K	D
4_bit Binary Counter	95	92	93
4_bit Shift Register Counter	96	95	95
4_bit Serial Data Transfer	90	93	92
4_bit Paralell Data Transfer	96	95	94

Table 2 shows the normalized delay time of the4 proposed technique as compared with the conventional design for the same conditions of supply voltage and transistor width.

Table 2. Normalized delay time, in %

FF-type	S/R	J/K	D
4_bit Binary Counter	89	90	93
4_bit Shift Register Counter	87	92	94
4_bit Serial Data Transfer	88	91	92
4_bit Paralell Data Transfer	89	90	90

From the above results it is clearly seen that the proposed technique using multi-threshold voltage achieves high-speed operation with low-power consumption at a low supply voltage of 1.8 V. Table 3 shows the SPICE parameters of the multi-threshold voltage technology used in our simulation are shown in Table 3.

Table 3. SPICE Parameters

Type:	Higt-V_{TH}	Low-V_{TH}
Gate Length	0.55 μm	0.65 μm
Gate Oxide Thickness	110 A	110 A
N-Channel:V_{TH}	0.55V8	0.25V
P-Channel:V_{TH}	$-$0.65V8	$-$0.35V

7 CONCLUSIONS

A new flip-flop implementation based on multi-threshold voltage techniques has been proposed in this paper, achieving high-speed operation with low power requirements. High threshold voltage transistors are used as non-critical path transistors, while low threshold voltage transistors are used in the critical path transistors to increase the operation speed of the circuit and at the same time reduce the power dissipation of the circuits. The parameter of transistor width has been fixed for all simulations of the conventional design and the proposed one as well. In each of the cases under consideration, the proposed technique has shown improvement in terms of power consumption over conventional techniques.

References

[1] CHANDRAKASAN, A., *et al*: A Low-Power Chipset for a Portable Multimedia I/O Terminal, IEEE Journal of Solid-State Circuits, 1415- 1428, December 1994.

[2] SHENG, S., *et al*: A portable multimedia terminal,, IEEE Commun. Mag. **30**, 64-75, Dec. 1992.

[3] MEINDL, J. D.: Low Power Microelectronics, Retrospect and Prospect, Proceedings of the IEEE, 619-635, April 1995.

[4] CHANDRAKASAN, A. P.—SHENG, S.—BRODERSEN, W.: Low-Power CMOS Digital Design, IEEE Journal of Solid-State Circuits, 473-484, April 1992.

[5] DAVARI, B.—DENNARD, R.: CMOS Scaling for High Performance and Low-Power - The Next Ten Years, Proceedings of the IEEE, 595- 606, April 1995.

[6] LIU, D.—SVENSSON, C.: Trading Speed for Low Power by Choice of Supply and Threshold Voltages, IEEE Journal of Solid-State Circuits, 10-17, January 1993.

[7] SUN, S. W.—TSUI, P. G.. Y.: Limitation of CMOS Supply- Voltage Scaling by MOSFET Threshold-Voltage Variation, IEEE Custom Integrated Circuits Conference, 267-270, 1994.

[8] MUTOH, S.— DOUSEKI, T., *et al*: 1-V Power Supply High-Speed Digital Circuit Technology with MultithresholdVoltage CMOS, IEEE Journal of Solid-State Circuits, 847-854, August 1995.

[9] MUTO, S., *et al*: A 1V Multi-Threshold Voltage CMOS DSP with an Efficient Power Management Technique for Mobile Phone Application, IEEE International Solid-State Circuits Conference, 168-169, February 1996.

[10] LIDSKY, D. B.—RABAEY, J. M.: Low-Power of Memory Intensive Functions, IEEE Symposium on Low Power Electronics (1994), 16-17.

[11] MORIMURA, H.—SHIBATA, N.: A 1-V SRAM for Portable Equipment, International Symposium on Low Power electronics and Design, 61-66, August 1996.

[12] BALABANIAN, N.—CARLSON, B: Digital Logic Design Principles, John Wily& Sons, Inc. 2001.

[13] TAKASHIMA, *et al*: Standby/Active Mode Logic for Sub-1 V, Operating ULSI Memory, IEEE Journal of Solid-State Circuits **29** No. 4, 441-447, April 1994.

[14] DATE, *et al*: 1-V 30-MHz 4-mW 2-mm2 16-b DSP Core,, ISSCC Dig. Tech. Papers, 84-85, February 1995.

[15] ALIDINA, M.—MONTEIRO, J.—DEVADAS, S.—GHOSH, A.: Precomutation-Based Sequential Logic Optimization, Proceedings of the International Conference on Computer-Aided Design, 74-81, November 1994.

[16] Computer Organization and Design, M. Mano, Printce-Hall, 1998. http://www.hyper-phecycs.comc.

[17] MENG, T. H.—GORDON, B.—TSERN, E.: A Portable Real-Time Video Decoder for Wireless Communication.

[18] KANG, S.: Accurate simulation of power dissipation in VLSI circuits, IEEE Journal of Solid-State Circuits (1986), 889-891.

Received 7 April 2003

Abdoul Rjoub received the Diploma and PhD degree in Computer Engineering and information, from Patras University, Patras, Greece, in 1994 and 2000, respectively. In September 2000, he is joined the Department of Computer Engineering, in Jordan University of Science and Technology, Irbid, Jordan. His present research interests include Low Power Design System, VLSI Design Architecture, and Parallel Design and Architecture.

Ali Shatnawi received the BSc and MSc in electrical and computer engineering from the Jordan University of Science and Technology in 1989 and 1992, respectively; and the PhD degree in electrical and computer engineering from Concordia University, Canada, in 1996. He has been on the faculty of the Jordan University of science and Technology since 1996. He is presently on a leave and working as the dean of Information Technology in the Hashemite University, Jordan. His present research covers hardware design, high level synthesis of DSP applications, VLSI realization, algorithm design, and wireless networks.