Design of a Micro Power Amplifier for Neural Signal Recording

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Abstract—This paper describes a micro power amplifier for neural signal recording. We describe an amplifier using a differential pair as input stage. Given that neural amplifiers must include differential input pair to achieve a high common-mode rejection ratio (CMRR). The amplifier has been designed in the AMS 0.35 μm, 3-metal, 2-poly, n-well standard CMOS process. The amplifier current consumption is 4.61 μA at ±1V supply, which gives a power consumption of 9.22 µW. The CMRR is 113 dB and the power supply rejection ratio (PSRR) > 73dB. The input referred noise is 14.8 µVrms over 100 ~ 10 KHz. The amplifier gives an input DC offset of 196 µV and an output swing of ±0.8 V with minimum distortion.

Key words—Neural signal recording, micro power amplifier, low noise, gain, CMRR, DC offset.

I. INTRODUCTION

The human central and/or peripheral nervous system has been a subject of study and fascination of the neuroscience and biomedical engineering communities for many decades. The neural signal recording has been an important research issue and is widely considered as key topics for better understanding, controlling and eventually restoring neurological functions using implantable microsystems. These one require a long term simultaneous recording of neural activity from many neurons simultaneously. The ideal system for long term recording would be a fully implantable device which is capable of amplifying the neural signals and transmitting them to the outside world [1], [2], [3].

Extracellular neural action potentials are one of the most challenging ones to record. They contain frequency components from 0.1 ~ 10 kHz and amplitudes in 50 ~ 500 μV range [4]. These signals usually carry DC baselines up to 500 mV due to electrode electrolyte interactions. The low-level signal amplitude, wide frequency range, and large DC baseline are the major challenges one would face when designing neural recording amplifiers. In addition, robustness of the amplifier in order to guarantee its proper operation in spite of the process and ambient variations is a major requirement. Further, it would be useful to have a robust amplifier with tunable bandwidth as well as variable gain that could be used for different types of biopotential signals or different components in one type of signal [4].

The most critical block in neural recording system is low-power low-noise neural amplifier which is the first stage in the neural recording system. There have been considerable research efforts in the design of low-power low-noise neural amplifiers in recent years. Harrison et al. described a low-noise low-power single-ended operational transconductance amplifier (OTA) with capacitive feedback for neural recording applications [5].

Although bioamplifiers that retrieve weak bioelectrical signals have been developed extensively [5]-[11], very few reported designs meet the noise, power, and size requirements for massive integration in implantable multichannel recording devices. Furthermore, the integrated designs that have been proposed give a high CMRR and a low power dissipation for safe permanent usage with an acceptable input referred noise.

The architecture of the neural recording system is discussed in Section II followed by the theoretical study of the neural amplifier in Section III. Section IV provides simulation results and Section V is the conclusion.

II. NEURAL RECORDING SYSTEM ARCHITECTURE

The block diagram of the neural recording signal is shown in fig. 1. It consists of tow units: an implantable transmitter and an external receiver unit. The implantable transmitter acquires neural signals from microelectrode array, amplifies, process and transmits them to external unit wirelessly through a miniature antenna. The receiver picks up the neural signal, digitizes it, and transfers it to external unit wirelessly. The implantable part is supplied by power and data via inductive link, not included in fig.1 [12].
III. THEORETICAL STUDY

A. Small signal analysis

In the small signal analysis, we focus only on the input differential stage. Fig.2 (a) and fig.2 (b) show respectively the transistor differential stage and the simplified equivalent diagram of the differential stage.

It notes that \( g_{m_i} \) is the transconductance of the transistor \( M_i \), with \( i=\{1, 2…7\} \).

B. Setting of equation

From the small-signal equivalent circuit (see fig.2(b)), we calculate:

\[
V_a = -g_{m_1}V_1 - \frac{1}{g_{m_4}} g_{m_2} V_2 - \frac{1}{g_{m_4}} g_{m_5} V_5
\]  
\( (1) \)

and

\[
V_s = -g_{m_2}V_2 - \frac{1}{g_{m_4}} g_{m_5} V_5
\]  
\( (2) \)

We obtain a relation between the differential output voltage \( (V_a - V_s) \) and the differential input voltage \( (V_2 - V_1) \) given by:

\[
V_a - V_s = \frac{g_{m_1}}{g_{m_4}} (V_2 - V_1)
\]  
\( (3) \)

With

\[
g_{m_1} = g_{m_2} = g_{m_3}
\]  
\( (4) \)

\[
g_{m_4} = g_{m_5} = g_{m_6}
\]  
\( (5) \)

\[
g_{m_7} = g_{m_8} = g_{m_9}
\]  
\( (6) \)

And

\[
k = \frac{g_{m_1}}{g_{m_4}} = \frac{g_{m_2}}{g_{m_4}} = \frac{g_{m_3}}{g_{m_4}}
\]  
\( (7) \)

C. Neural amplifier circuit analysis

Fig.2 shows the schematic of the neural recording amplifier which composed of a differential stage and an output gain stage.

If \( k > 1 \); the structure given by fig.3 works as a hysteresis comparator.

If \( k < 1 \); therefore, it works as a differential amplifier, and for maximum voltage gain, \( k \) must tend to 1, and \( g_{m_1} \) must be very large compared to \( g_{m_6} \).

By operating the transistors \( M_1 \) and \( M_2 \) in weak inversion, we can simplify the equation (3) to :

\[
V_a - V_s \approx \frac{1+k}{1-k} (V_2 - V_1)
\]  
\( (8) \)

Referring to fig.3, we can express the output voltage \( V_{out} \) in terms of the differential amplifier input:

\[
V_{out} = V_{g} g_{m_1} R_{out} - V_{g} g_{m_5} R_{out}
\]  
\( (9) \)

With \( R_{out} \) is the amplifier output resistance, and \( g_{m_6} \), \( g_{m_9} \) are the respective transconductance of transistors \( M_8 \) and \( M_9 \). Following a small-signal study of the output stage, we calculate the output resistance as follows:

\[
R_{out} = (rds_{g} g_{m_1} rds_{13}) / (rds_{12} g_{m_6} rds_{13})
\]  
\( (10) \)

Consider the case where \( g_{m_6} = g_{m_9} \), and from equations (8) and (9), we obtain an output voltage as:

\[
V_{out} \approx g_{m_6} R_{out} \frac{1+k}{1-k} (V_2 - V_1)
\]  
\( (11) \)

D. Technological specification

In order to realize a low power and low noise amplifier, to amplify neurological signals which have low amplitude (from 50 to 500μV). We must respond to technological specifications and requirements listed in Table I.
### TABLE I
**SPECIFICATIONS AND REQUIREMENTS**

<table>
<thead>
<tr>
<th>Specifications and requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology AMS 0.35μm</td>
</tr>
<tr>
<td>Supply voltage ±1V</td>
</tr>
<tr>
<td>Gain</td>
</tr>
<tr>
<td>Gain bandwidth</td>
</tr>
<tr>
<td>Phase margin</td>
</tr>
<tr>
<td>Power consumption</td>
</tr>
<tr>
<td>Common Mode Ratio Rejection CMRR</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio PSRR</td>
</tr>
<tr>
<td>Load capacitance</td>
</tr>
</tbody>
</table>

### IV. SIMULATION RESULTS

Referring to fig.3 and respecting the specifications and the requirements shown in table 1, we calculate the size of different devices. Table 2 presents the parameters values of the neural recording amplifier.

#### TABLE II
**NEURAL AMPLIFIER PARAMETER VALUES**

<table>
<thead>
<tr>
<th>Devices</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M2</td>
<td>W=100µm L=1µm</td>
</tr>
<tr>
<td>M3, M10, M11, M12, M13, M18, M14</td>
<td>W=1.5µm L=1µm</td>
</tr>
<tr>
<td>M4, M5, M8, M9, M15, M16, M17</td>
<td>W=6µm L=1µm</td>
</tr>
<tr>
<td>M6-M7</td>
<td>W=5µm L=1µm</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>Vdd=1V Vss=-1V</td>
</tr>
<tr>
<td>Load capacitance</td>
<td>C_L=7pF</td>
</tr>
<tr>
<td>Bias current</td>
<td>I_bias =1µA</td>
</tr>
</tbody>
</table>

By using Pspice, we process to simulate the circuit given by fig.3. We determine various characteristics such as gain, phase margin, power, noise, CMRR, PSRR, and offset.

- **Frequency analysis**

We apply an AC source in the input of the amplifier given in fig.3. The schema in fig.4 is used to draw the Bode diagram and to extract its dynamic characteristics.

![Fig.4: AC simulation](image)

Fig.5 shows the Bode diagram that gives a gain=43.95 dB (equivalent to 157.57). The phase margin is equal to 64.6°, hence the stability of the system. The gain-bandwidth is GBW = 1.1294MHz.

- **Noise analysis**

The input-referred noise voltage of CMOS amplifier is dominated by flicker (1/f) noise at low frequencies and thermal/shot noise at higher frequencies. The frequency at which the noise tail intersects the noise floor is called the flicker-noise corner frequency. By representing the noise sources of each transistor by a voltage source at its input, the total input-referred noise contribution can be calculated by considering the voltage gains from the device to the amplifier output.

In order to examine the noise performance of neural amplifier, it was simulated using the Pspice. Fig.6 shows the input-referred noise voltage versus frequency.

![Fig.6: Simulated input-referred noise voltage](image)

The Root Mean Square (RMS) of the input-referred noise voltage: \( V_{n,rms} = 14.8 \mu V \text{rms} \) calculated for a frequency range 100Hz ~ 10 KHz. This value is competitive compared with other developed recording amplifiers reported in the literature [10], [13].

- **Noise Efficiency Factor**

We are interested in minimizing noise within a strict power budget; we must consider the tradeoff between power and noise. To compare the power–noise tradeoff among amplifiers, we adopt the noise efficiency factor (NEF) which is widely used to compare neural amplifier designs. The noise efficiency factor is expressed as:

\[
NEF = \frac{V_{n,rms}}{\sqrt{\text{BW}}^2} \cdot \frac{2I_w}{\pi U_T^2 K_B T \cdot \text{BW}}
\]  

(12)

Where \( V_{n,rms} \) is the total input-referred noise, \( I_w \) is the total supply current, and \( \text{BW} \) is the -3 dB bandwidth of the amplifier. \( U_T \) is the thermal voltage, \( K_B \) is the Boltzmann constant and \( T \) is the temperature.
For $U_T=25\,\text{mV}$, $T=27\,\text{°C}=300\,\text{°K}$, $K_B=1.3806.10^{-23}\,\text{[J/K]}$, $I_{\text{tot}}=4.617\,\mu\text{A}$, $V_{\text{n,rms}}=1.4888E-05\,\text{Vrms}$ and $BW=[100\,\text{Hz},10\,\text{KHz}]$.

We obtain $\text{NEF}=13.22$ which is competitive compared with [7].

- **Summary table**

Table III summarizes the simulation results of the neural recording amplifier.

| TABLE III  |
|------------------|------------------|
| **SIMULATED PERFORMANCE CHARACTERISTICS OF NEURAL AMPLIFIER** |
| **Parameters** | **Value** |
| Gain | $G_{\text{dB}}=43.95\,\text{dB}$ |
| Phase margin | $\Phi=64.6^\circ$ |
| Gain-BandWidth | $GBW=1.1294\,\text{MHz}$ |
| Power Consumption | $P_{\text{tot}}=9.22\,\mu\text{W}$ |
| Total Current absorbed | $I_{\text{tot}}=4.617\,\mu\text{A}$ |
| Common Mode Rejection Ratio | $\text{CMRR}=113.27\,\text{dB}$ |
| Power Supply Rejection Ratio | $\text{PSRR}_{\text{vss}}=73.11\,\text{dB}$ |
| Output-voltage swing | $\text{CMR}+=806\,\text{mV}$, $\text{CMR}=-992\,\text{mV}$ |
| DC Offset | $196\,\text{µV}$ |
| Input Referred Noise | $V_{\text{n,rms}}=14.8\,\mu\text{Vrms}$ |
| Noise Efficiency Factor | $\text{NEF}=13.22$ |

IV. CONCLUSION

This paper presents the design of an integrated micro-power amplifier for neural recording signal. The architecture of the neural recording system was discussed and followed by the theoretical study of the neural amplifier. Furthermore, PSpice simulation which using a real transistor model was presented. In particular, the transfer function of amplifier and the noise analysis were presented. A power dissipation of about 9.22 $\mu\text{W}$ and an input referred noise about 14.8$\mu\text{Vrms}$ were achieved. Future work will focus on the study of closed-loop amplifier with adjustable gain and low cut off frequency.

REFERENCES


