Design, Fabrication, and Test of CMOS Active-Pixel Radiation Sensors

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***Abstract*—In this paper, we discuss some issues related to the design, implementation, and test of a CMOS active pixel sensor chip (RAPS01), developed in the framework of the radiation active pixel sensors (RAPS) INFN project. Two different basic pixel schemes have been proposed. The first one is based on a standard active pixel sensor (APS) architecture, while a second architecture, named weak inversion pixel sensor (WIPS) exploits a different circuitry which allows for "sparse" access mode and thus for speeding-up the readout phase. Chip fabrication has been completed and a preliminary test phase has been performed. A suitable test environment has been devised and test strategies have been planned. Preliminary test results, featuring a static and dynamic characterization of the basic sensitive elements are outlined. Future works are also outlined, aimed at the optimization of a second version of the chip, more effectively integrating smart circuitry.**

***Index Terms*—Active pixel, CMOS, radiation sensor.**

I. Introduction

PROTOTYPES CMOS radiation sensors have been presented in the technical literature [1]–[4]: in this paper, we discuss design, implementation, and test issues related to the RAPS01 chip developed in the framework of the RAPS project supported by INFN (Italy). The project aims at assessing the feasibility of smart, high-resolution pixel arrays with a fully standard, submicron CMOS technology. This will require: physical evaluation of device fabrication technologies, with respect to charge collection performance; optimization of the sensitive element layout; pixel design, including local read and amplification circuits; system design, including array addressing, control, and I/O circuits. Active-pixel CMOS detectors are been routinely designed for different applications (e.g., digital cameras); the specific application described here poses functional and performance specifications which require a different design.

II. Technology Analysis

An analysis of state-of the-art, standard, and commercially available CMOS technologies was conducted. Numerical simulation [5] has provided an inexpensive and reliable instrument to estimate photodiode charge collection, depending on technology features such as substrate doping profile, presence of low-doped epi-layer, layout rules, etc. Device simulation has been exploited throughout the entire design phase: to achieve reasonable tradeoffs between physical accuracy and computational requirements. Mixed-mode (i.e., device/circuit) has been used to model distributed effects (charge collection, crosstalk) at the physical level and to account for the circuit shown in Fig. 1. Eventually, UMC 0.18-μm CMOS fabrication technology (6-metal, 1-poly, mixed-signal) was selected for the fabrication of the first prototype.

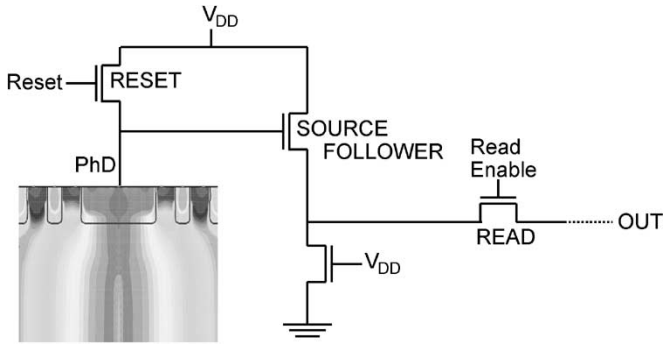

Fig. 1. APS basic circuit. Mixed-mode analysis: the photodiode response is modeled by physical device simulation, while further on-pixel signal handling is simulated by compact circuit models.

III. System Architecture

Specifications of particle detectors differ from conventional imaging applications since higher spatial resolution is desired and sparse hits over relatively large surfaces are to be covered (whereas limited-size pixel frames have to be periodically scanned in the more conventional case). This requires a quite different readout architecture, both at the pixel level and at the system control and I/O interface.

Two different basic pixel schemes have been proposed to solve this issue. The first one is based on a standard active pixel sensor (APS) architecture, shown in Fig. 1, and is aimed at optimizing both the spatial resolution and the signal-to-noise ratio (SNR). In particular, we looked for the optimization (with respect to the output voltage swing) of the dimensions of the sensitive element. The pixel layout was carefully designed, in order to balance sensitive volume and parasitic capacitance. Although the fabrication technology lacks an almost-intrinsic epi-layer [which may improve [2] charge-collection efficiency (CCE)], it features a relatively low-doped ($\mathrm{N} = 10^{15}\ \mathrm{cm}^{-3}$) bulk substrate, so that satisfactory CCE figures can still be obtained. ISE-TCAD [5] device-simulation package was used to estimate

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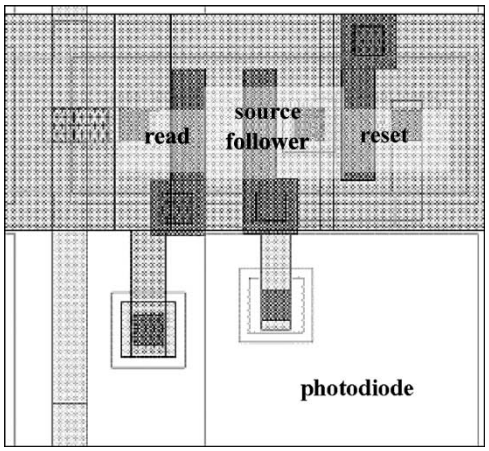

Fig. 2. APS pixel layout.

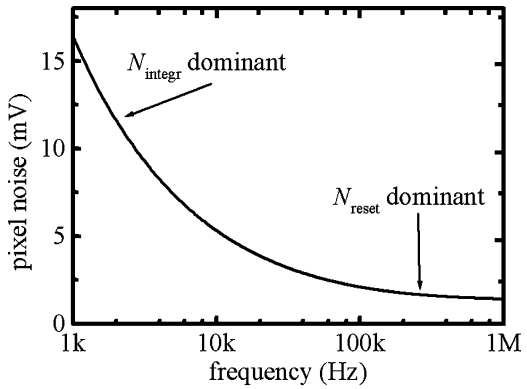

Fig. 3. Total pixel noise calculated for APS structure ($\mathrm{T} = 300\,\mathrm{K}$).

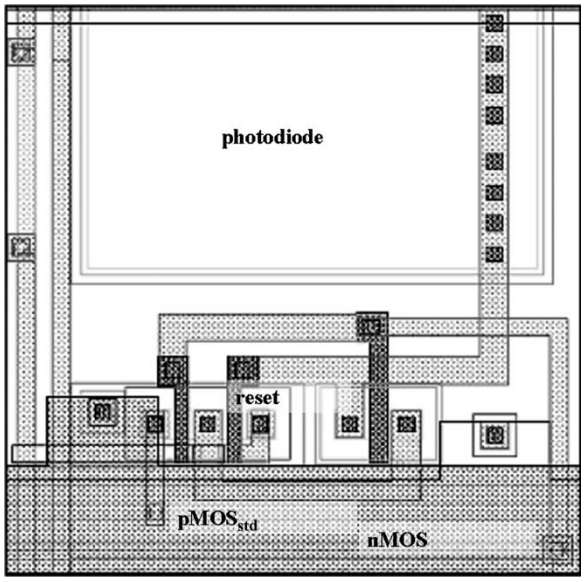

Fig. 4. WIPS pixel layout.

CCE: a value of about 570 collected electrons was found (for a particle hitting the center of a pixel detection area), close to literature data for epi-layer based pixels [2]. Assuming a typical generation rate of 80 electron-holes pairs per micron, this means that 90% of electrons generated in the first 8 $\mu\mathrm{m}$ of silicon depth are actually collected. Simulation shows that deeper layers do not contribute significantly to the collected charge. Thus, since charge sharing among adjacent pixels is limited, small pixel pitches (3.3 $\mu\mathrm{m}$, with a $2.2 \times 1.8\,\mu\mathrm{m}^2$ junction area) can be more effectively exploited. A layout view of APS pixel is shown in Fig. 2.

Simulation predicts voltage swing at the photodiode cathode in the order of several tens of mV. To estimate expected SNR, pixel noise has been calculated as well. The pixel-reset noise (N_{reset}) is determined by the thermal noise of the photodiode, and can be estimated [6] as

$$\overline{N_{\mathrm{reset}}^2} = \frac{1}{2}\frac{kT}{C} \tag{1}$$

where C is the capacitance seen at the photodiode node (PhD). Charge-integration noise (N_{integr}) is instead due to dark current (I_{dark}) and is approximately

$$\overline{N_{\mathrm{integr}}^2} = \frac{q \cdot I_{\mathrm{dark}} \cdot t_{\mathrm{integr}}}{C^2} \tag{2}$$

where t_{integr} is the charge-integration time. Total pixel noise is obtained from the root mean square (rms) of reset and charge-integration noises. Relative weight of noise components strongly depends on the actual working frequency, as shown in Fig. 3: assuming a 1-MHz reset frequency, with a 20% duty-cycle, total pixel noise should be around 1.4 mV.

The second architecture, named weak inversion pixel sensor (WIPS) is shown in Fig. 4, and is more explicitly conceived for a sparse access mode [7]. The readout circuitry is based on a precharge-evaluation scheme, whose operating principle is sketched in Fig. 5: through a RESET pulse, the photodiode is charged, raising photodiode (PhD) node voltage up to the point at which the $\mathrm{PMOS_{std}}$ device switches off. At the same time, row (A) and column (B) lines are precharged at high and low values, respectively. Then RESET goes down, and the photodiode is isolated. If a radiation hits the diode, $\mathrm{V_{FDT}}$ slightly decreases, $\mathrm{PMOS_{std}}$ switches on, and charge is allowed to flow through its channel. Charge sharing thus occurs between nodes A and B, allowing for identifying both hit column and row, with no need to probe sequentially each pixel in the matrix.

Circuit and device simulation has been extensively used to validate and characterize WIPS behavior: simulated response of both hit row and column output signals are shown in Fig. 6. The operating mode devised so far makes the sparse pixel readout more efficient. Assuming a pixel array having m rows and n columns, in order to find out a hit pixel, the conventional scheme requires scanning each pixel in the array, thus requiring a time proportional to $(n \times m)$. The WIPS scheme allows independent scanning of column and row outputs, so that time becomes proportional to $(n + m)$. Mean power dissipation follows the same trend, as shown in Fig. 7.

A potential drawback of the WIPS scheme is the introduction of pMOS devices into the active pixel; the n-well junction actually may act as a parasitic charge drain, competing with the photodiode. To minimize such effect, a large area ratio between the photodiode and the pMOS footprints has been imposed, thus resulting in a larger pixel than in the previous case. The layout of a complete WIPS pixel is shown in Fig. 4: by using device simulation in this case too, device geometry has been optimized, with respect to CCE, capacitance and influence of the parasitic

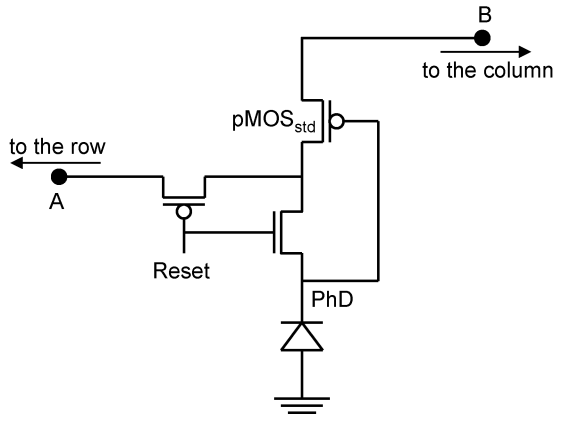

Fig. 5. WIPS pixel circuit.

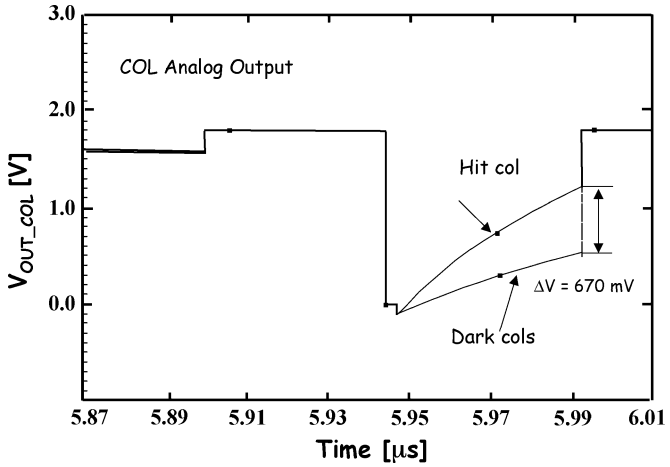

Fig. 6. WIPS simulated response.

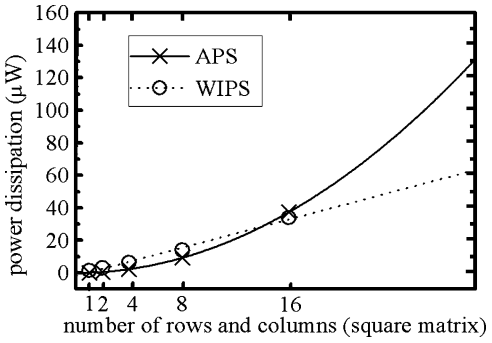

Fig. 7. Matrix power dissipation for APS and WIPS structures. Readout times follow the same trend.

junction [7], eventually resulting in a $(7.5\times4.7\,\mu\mathrm{m})$ photodiode area, and an overall pixel pitch of 10.3 μm.

IV. Chip Fabrication

Although simulation provides useful information, experimental validation and comparison of different architectures is still of the utmost importance to verify and to select the most suitable architecture for a detector. This is required since the CMOS technology has not been developed or characterized by the foundry for radiation sensor applications. Therefore, once basic architectures of the pixel array have been defined, fabrication of a prototype chip, conceived for test and validation, has been planned. A numbers of test devices, ranging from single-pixel to small (yet functionally complete) pixel arrays have been placed on the chip floorplan. Separate testing of all functional blocks (e.g., amplifier stages) has been provided. Different pixel layouts have been considered, as well as different matrix geometries (by varying pixel number and pitch). Some relevant technology options have been considered: alternative solutions have been investigated for the implementation of sensitive elements, e.g., either using a twin-tub layer or optionally "blocking" the p-well layer. Since junction capacitances have a strong influence on the SNR, this may play a significant role in setting charge collection efficiency and minimum resolution. For the same reason, arrays featuring different substrate biasing schemes (e.g., adopting guard-ring structures at each pixel) have been implemented. Random access to each pixel has been foreseen for testing purposes; by implementing dedicated row and column decoders, and both analog and digital output channels have been implemented. Fig. 8 shows a view of the actual fabricated chip: it includes 11 APS arrays, 8 WIPS arrays, and several simpler test structures. Due to the wide variety of integrated devices to be independently controlled and considering power supply constraints (1.8 V, both analog and digital, and digital 3.3-V power supply voltages have to be provided to the chip), an exceedingly large number of signals would have to be exported at the chip I/O pins. To circumvent this problem, two different bonding schemes are applied to a JLCC84 case, each one allowing for accessing a subset of the integrated structures. Chip fabrication has been completed, in a multiproject wafer (MPW) framework, and preliminary tests have been performed, as illustrated next.

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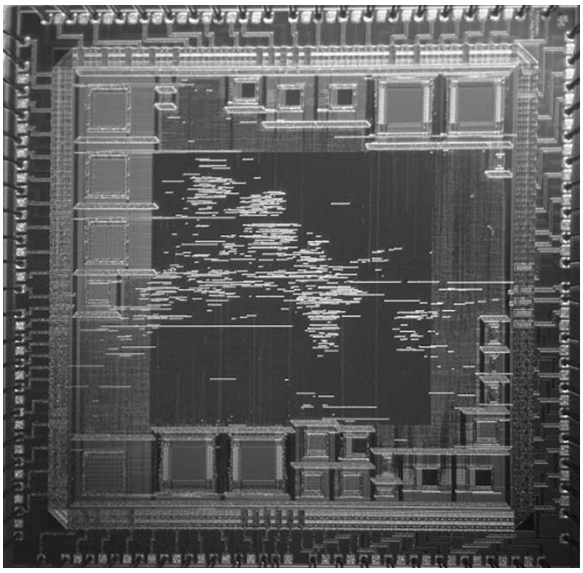

Fig. 8. RAPS01 chip microphotography.

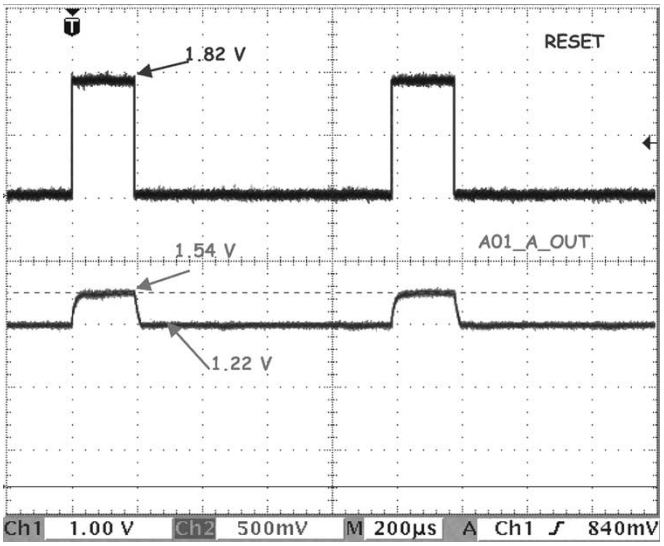

Fig. 9. APS dark condition response.

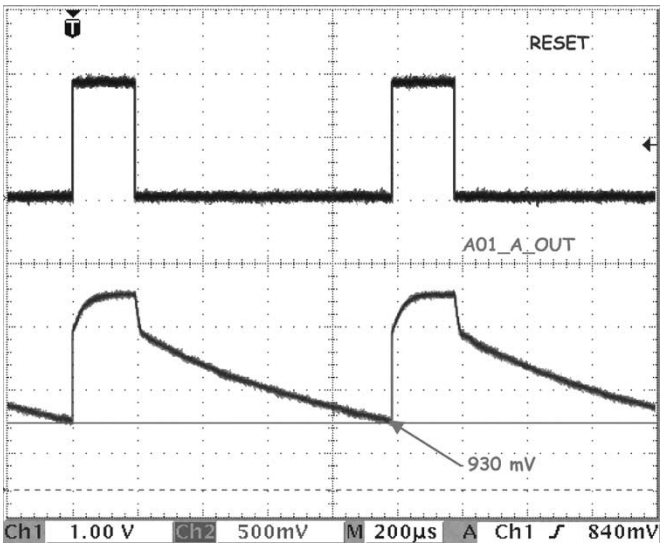

Fig. 10. APS light condition response.

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V. Chip Test

As previously discussed, several test structures have been integrated on the RAPS01 chip, ranging from stand-alone photodiode response to complete readout circuitry: this results in a fairly articulated sequence of test signals to be generated and delivered to the chip. For this purpose, a dedicated printed circuit board (PCB) has been designed and fabricated: from the functional point of view, maximum flexibility has again been pursued, accounting for both manual and automatic test procedures. All of the control and I/O signals can be generated either through on-board hardware circuitry or at the software level, by means of LabView routines driving the test board from a PC.

To begin with, the dark response of a single APS matrix has been evaluated. A periodic reset signal was sent to the whole matrix under test: the corresponding analog output at a single pixel is reported in Fig. 9; feedforward capacitances of the reset transistor are responsible for the changes of the output. Then, the whole chip was illuminated: to allow for optical test, coverage of sensitive areas with metal layers was actually avoided in the chip design. A much larger decrease of the output voltage was experienced, in this case, during the "read" phase (Fig. 10). However, amplitude and time response strongly depend on the output amplifier stages. Bias point of such amplifiers is critical, since no measures of the test structures were available at design time, and, as stressed earlier, a large uncertainty affected estimated results. Digital programming of the amplifiers bias point was accounted for in the chip design, allowing for *a posteriori* fine-tuning of the operating point. A 15-bit string encodes the configuration data, and is sequentially uploaded to the chip before starting operation. Sensitivity of the output signals to such preconditioning is illustrated by the white-light responses in Figs. 11 and 12. Fig. 11 refers to a nonoptimal amplifier configuration, whereas Fig. 12 shows optimized response: the improvement is quite evident, both in terms of signal amplitude and time-constants. Improved performance can consequently be obtained at the digital outputs as well, as reported in the same figures. A more detailed circuit analysis goes beyond the scope of this paper; it is worth stressing that configuration capability makes the test phase more flexible and tolerant, and gives useful hints for optimization [7] of next-generation chip. Then, the system response to ionizing particles was checked

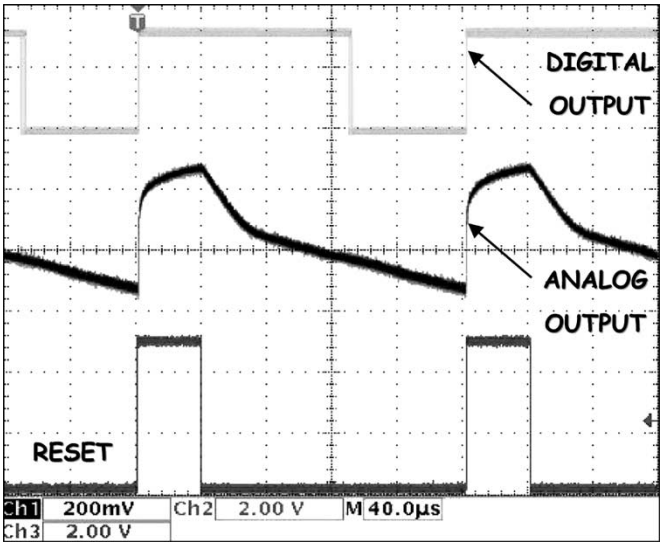


Fig. 11. APS response, nonoptimized amplifier configuration.

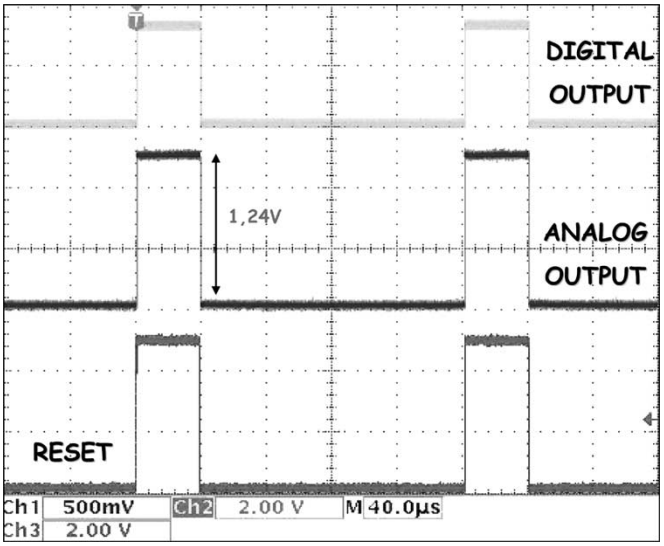


Fig. 12. APS response, optimized amplifier configuration.

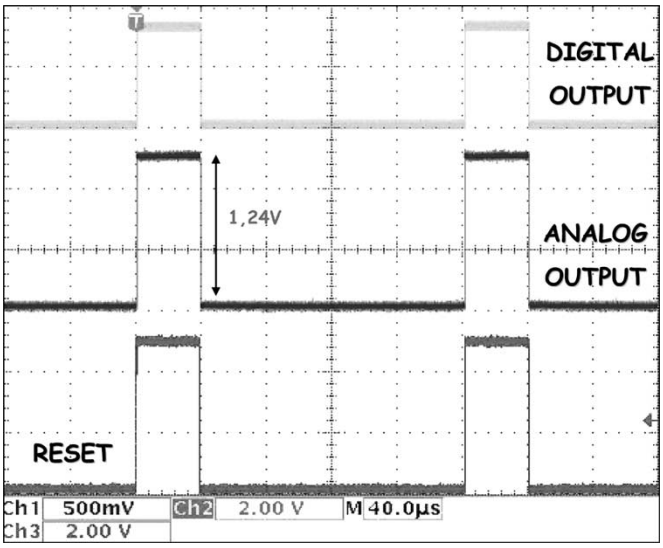
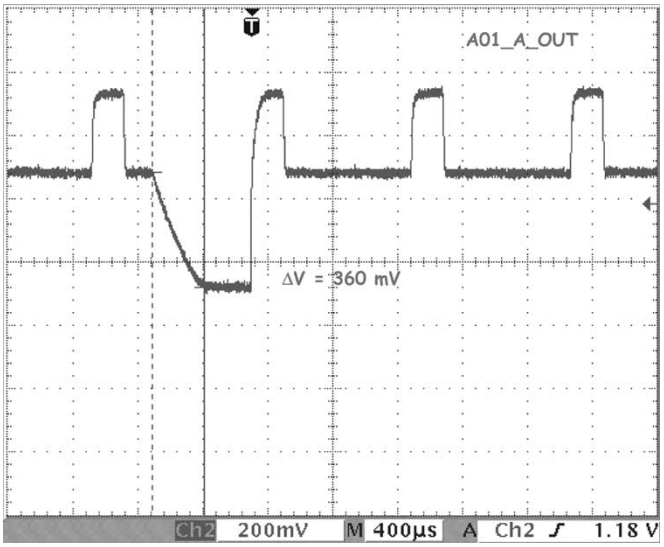


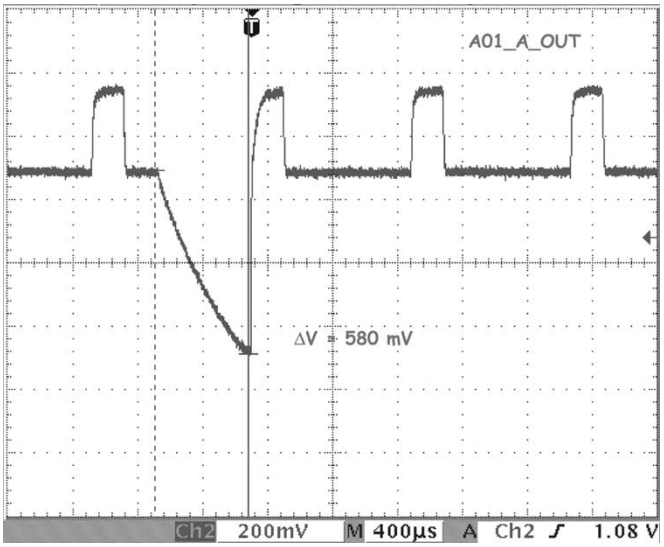
Fig. 12. APS response, optimized amplifier configuration.

using an Americium α-source, which is closer to the high-energy physics environment. Time-domain pixel responses to the α-particle hit are reported in Fig.13(a) and (b), for two different events. Differences in the impinging particle energy are discriminated by the analog output, which exhibits a quite appreciable voltage drop.

Similar tests are being conducted on WIPS devices. Since WIPS share the same fabrication technology of APS devices tested so far, basic performance of photodiodes should not differ radically (influence of parasitic junctions has been minimized in the design phase). An issue that nevertheless it is worth mentioning here is that of leakage currents: since the basic scheme of WIPS devices relies on a control transistor biased on the conduction onset, leakage current may become a concern for arrays larger than those actually implemented in the RAPS01 chip. This however, can be solved by properly partitioning the interconnection arrays in several subsections; alternatively, a much larger swing (and thus much lower leakage currents in the off-state) at the control gate of the pass-transistor can be



(a)



(b)

Fig. 13. (a) APS α-particle stimulus response. (b) APS α-particle stimulus response.

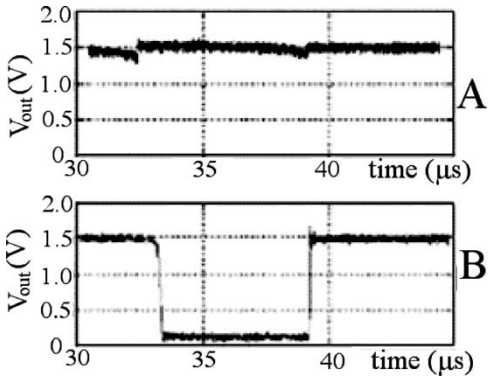


Fig. 14. WIPS light stimulus response: digital output for dark condition (A) and illuminated pixel (B) (please note that digital encoding of different, i.e., opposite, from APS one).

obtained by accounting for on-pixel voltage amplification. Different pixel architectures extending the WIPS approach have been devised and will be implemented in next silicon run. Here, however, our primary goal was the validation of the basic operating principle of the pixel readout scheme. Fig. 14 refers to the digital output of the WIPS pixel, and compares dark (A) and light (B) responses. Full functionality of the WIPS approach is, hence, assessed; a more extensive characterization will be soon completed and discussed elsewhere.

Beside the preliminary chip measurements discussed in this paper, a more complete set of measurements is being carried in order to evaluate pixel response homogeneity and matrix sensibility, as well as more precisely SNR, power consumption, and spatial resolution.

VI. Conclusion

The design of RAPS01 chip was primarily aimed at the validation of basic performance of sensitive elements integrated in standard CMOS technology for particle detection. Preliminary test have been carried out on an active pixel sensor fabricated in a 0.18-μm CMOS technology. The suitability of such an approach, in particular the adoption of a standard CMOS substrate with optimized pixel layout, has been verified. Preliminary results are very encouraging: a significant SNR, expressed in terms of output voltage drop, has been obtained for both optical (white light) and α-source stimuli. Accounting for suggestions coming from RAPS01 test results the realization of a second chip (RAPS02) is foreseen, aiming at global performance tuning, more effective exploitation of sparse-readout features and integration of on-chip signal processing capability.

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